THERMO-MECHANICAL RELIABILITY OF ULTRA-THIN LOW-LOSS SYSTEM-ON-PACKAGE SUBSTRATES

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THERMO-MECHANICAL RELIABILITY OF ULTRA-THIN LOW-LOSS SYSTEM-ON-PACKAGE SUBSTRATES

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To my Mother - thanks for always walking beside me.

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SUMMARY

Miniaturization and functionality have always governed advances in electronic system technology. To truly achieve the goal of a multi mega-functional system, advances must be made not just at the IC level, but at the system level too. This concept of tighter integration at the system level is called System-on-Package (SOP). While SOP has a wide range of applications, this work targets the mobile application space. The main driver in the mobile application space is package profile. Reduction in thickness is very critical for enabling next-generation ultra-high density mobile products. In order to pack more functionality into a smaller volume, it is absolutely imperative that package profiles are reduced. The NEMI roadmap projects that the package profile should be reduced to 200µm from the current 500µm by 2014.

This work attempts to demonstrate the feasibility of ultra-thin substrates (<200µm) using a new advanced material system tailored for high-frequency mobile applications.

The main barriers to adoption of thin substrates include processing challenges, concerns about via and through hole reliability and warpage. Each of these factors is studied and a full-fledged test vehicle built to demonstrate the reliability of thin substrates using the advanced low-loss RXP-4/RXP-1 material system. Finite element models are developed to provide an understanding of the factors that affect the reliability of these substrates. Finally, IC assembly is demonstrated on these substrates.

CHAPTER 1

INTRODUCTION

This chapter deals with the motivation for the move to thin substrates and the challenges that arise as a result. The electrical and thermo-mechanical advantages of thin substrates are discussed. The challenges in processing these substrates and ensuring reliability are also discussed. Finally, the research objectives and thesis outline are presented. This work was done as part of System-on-Package research at Packaging Research Center, Georgia Institute of Technology.

Miniaturization and functionality have always governed advances in electronic system technology. Traditionally, IC downscaling in accordance with Moore's law has been used to accomplish this goal. However, Moore's law only deals with 10% of the system. The other 90% consisting of passives components such as resistors, capacitors and inductors are still present and preclude the possibility of further miniaturization [1]. To truly achieve the goal of a multi mega-functional system, advances must be made not just at the IC level, but at the system level too. This concept of tighter integration at the system level is called System-on-Package (SOP). With the aid of this two-pronged strategy of shrinking both IC and system levels, the goal of multi mega-functional systems can be achieved. SOP enables highly miniaturized heterogeneous integration of RF/digital/opto/sensing functions by system-centric IC-package codesign and functional optimization with 3D integration of thin film components between the ICs and package. The focus of SOP is thus on miniaturization of system components, including not only

actives, but also passives, power sources, I/Os, thermal structures, and system I/Os. With this fundamentally new paradigm, the SOP methodology overcomes the barriers of System-on-Chip (SOC) leading to cheaper and faster-to-market convergent microsystems. SOP is expected to enable electronic devices to achieve unprecedented functionality and miniaturization at reduced cost. Figure 1.1 shows a schematic of the SOP concept.

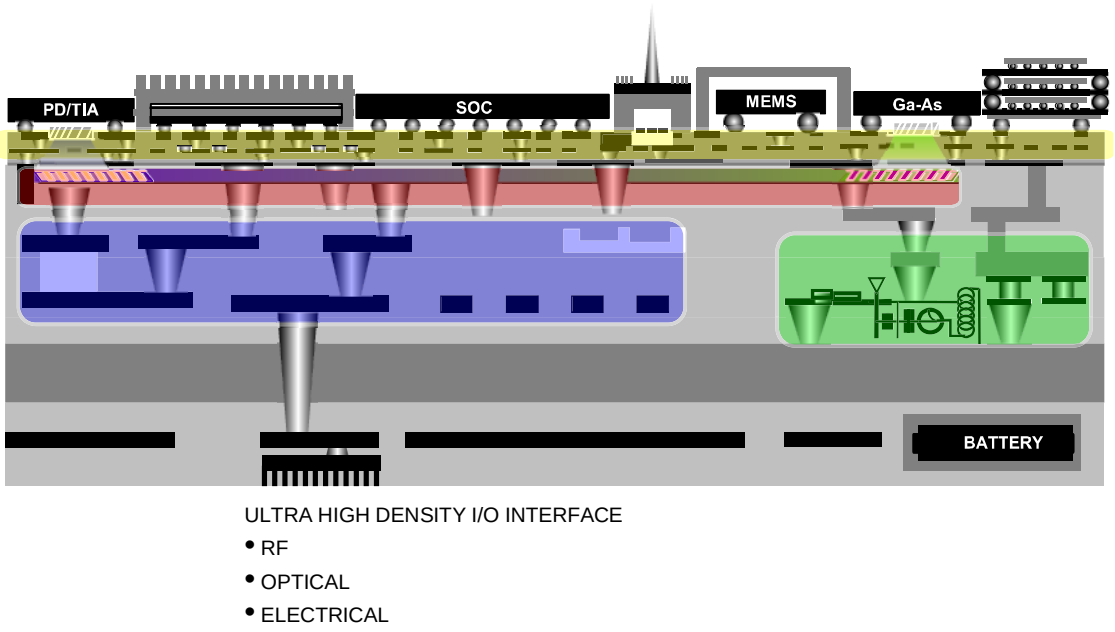


Figure 1.1 Schematic of SOP concept

1.1. Drivers and Motivation for Research

While SOP has a wide range of applications, this work targets the mobile product application space. The main system trend in mobile products is higher function density (# of functions per unit volume) and this in turn drives miniaturization of packages and modules. In addition to X-Y size reduction, the reduction in thickness is very critical for enabling mega-functional density for next generation mobile products. This package profile reduction can be achieved by thinning silicon devices, shorter IC-to-package and

package-to-board interconnects. However, one of the most effective methods for thin packages is to replace current thick package substrates (0.5-1.0+mm thickness) with ultra-thin (<0.2mm) and high density substrates.

The other significant change in mobile devices in recent years is the increasing use of wireless communication and the need for higher and higher frequency of operation. High frequency performance in the multiple-GHz range requires dielectric materials with outstanding electrical properties in terms of dielectric constant and loss [2].

Apart from the above factors, two other critical parameters required for advancing mobile technology are microvia and through hole diameters. To support the spiraling need for higher wiring density, it is imperative that microvia and through hole diameter/pitch are reduced. Table 1.1 summarizes the current state-of-the-art and projected roadmap values for some key properties of package substrates. This data was obtained from the NEMI and ITRS roadmaps.

Table 1.1 Current and future trends in the mobile application space [3, 4]

	2008	2014
Substrate Profile	0.5 mm	0.2 mm
Dielectric constant/loss	3.1/0.012	2.5/0.002
Via Diameter	50µm	25µm
Through Hole Diameter	70µm	40µm

As can be seen from the table, profile reduction of 200µm needs to be achieved by the year 2014. This entails the move to thinner substrates which means that the thickness of the core and the build-up material need to be reduced. Furthermore, new materials and processes need to be developed which can support the performance required in the future. Materials research needs to be followed closely by process research, given that the new material could be vastly different from the conventionally used epoxy material.

1.2. Advantages of Thin Substrates

Thin substrates possess a number of advantages. As discussed previously, more functionality can be packed in a given volume. This would translate to including in the same volume, the features of a phone and a GPS for example, where previously it would only have been possible to include the features of a phone.

The use of thinner dielectrics in these substrates means that smaller microvias can be made for Z interconnections. Microvia diameters have a direct dependence on the thickness of the dielectric. It is difficult to produce high-aspect ratio microvias. Reduction of dielectric thickness would help in producing smaller microvias and consequently higher wiring density. Also, shorter interconnections are more reliable, making them more attractive. Electrical performance is also improved by using thin substrates. Thinner dielectrics can supply lower impedance values. Signal integrity is also improved by using thinner substrates.

1.3. Current State-Of-The-Art

The current standard in substrate technology consists of Bismaleimide triazine (BT) core and Ajinomoto Build-up Film (ABF) as build-up dielectric [5-7]. While these materials have provided good performance with excellent reliability, there are limitations in terms of performance with the move to higher frequencies and lower dielectric constant. The dielectric constant of ABF is 3.1-3.3 with a loss tangent of 0.012. Table 1.1 indicated the need for materials with low dielectric constant < 2.5 with a loss tangent < 0.002. Further, ABF has been reported to crack when laminated on cores with thickness < 500µm. These limitations necessitate the need for new loss-loss materials which can be incorporated in ultra-thin package substrates.

1.4. Research Challenges for Low-loss Ultra-Thin Substrates

Reducing the thickness of the substrate using advanced materials to attain lower profile thicknesses poses a number of challenges. The need for improved material properties places further demands in terms of process research on these new materials. Some of these challenges are listed below and discussed:

Via and Micro Through Hole (MTH) Reliability Challenge

The reliability of microvias and micro through holes (through holes with diameter < 100µm) is an area of concern at these thicknesses. While a number of researchers have studied via reliability [8-12], the effect of substrate thickness is not well documented. It

might be expected that the thinness of the substrate should lead to increased reliability [13], but this has to be confirmed.

Warpage Challenge

The low stiffness of the substrate can lead to very high warpage in the substrate. Warpage has the following effects on substrate processing and reliability:

1. *Coarser feature size:* Warpage limits the lithographic capabilities by improper mask alignment and optics of the exposure. This means that the designer can only use coarser features in his design.

2. *Via-pad misalignment:* Package designers incorporate misregistration from layer to layer in multilayered thin film structures with larger capture pads for vias. Higher warpage requires larger capture pads for the vias thus reducing wiring density. Figure 1.2 shows a schematic of this effect.

3. *Assembly:* High warpage will lead to greater assembly stresses during reflow and could lead to bridged solder joints [14]. Defects observed during assembly are almost entirely dependent on package warpage. The warpage of the bare substrate should be < 4 mils for successful and reliable assembly [14, 15].

4. *Processing Challenge:* The use of advanced materials requires extensive process research. Optimization of various processes is required before a new material can successfully be used to build high density substrates.

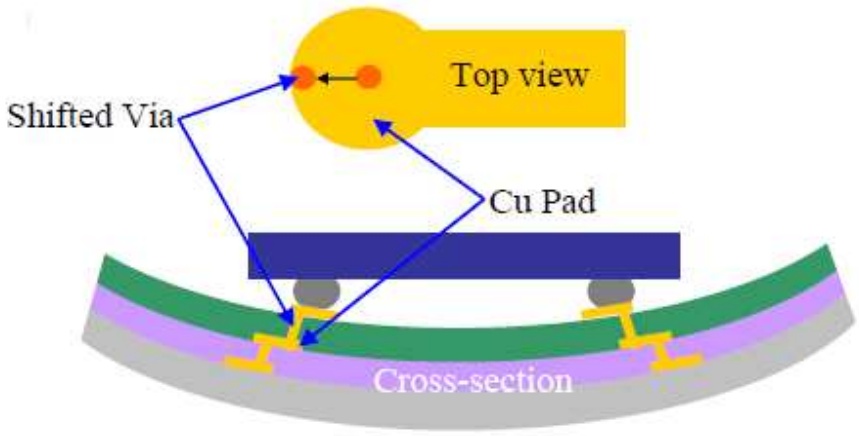


Figure 1.2 Via-pad misregistration as a result of warpage [16]

1.5. Objectives of current research

1. Understand thermo-mechanical reliability of ultra-thin low loss substrates through finite element modeling in two main aspects:
    a. Microvia reliability
    b. Warpage
2. Explore and demonstrate 4 layer ultra-thin substrate with microvias and micro through holes consistent with the roadmap targets outlined previously.

3. Demonstrate fine-pitch assembly capability and substrate reliability (with microvias and micro through holes) on four metal layer ultra-thin substrates with <200um thickness.

1.6. Thesis Outline

This work studies a number of factors that influence the adoption of ultra-thin substrates. A full-fledged test vehicle is built to demonstrate the feasibility of these substrates.

Chapter 2 describes the processes developed on the advanced low-loss RXP-4/RXP-1 materials system. The fabrication of the test vehicles is also described. Testing procedures that were used to ascertain reliability are then described.

Chapter 3 describes the finite element models that were developed for understanding microvia reliability and warpage. The geometry, material models and loading conditions are described.

Chapter 4 presents the results. Both experimental and FE results are described in this section. Chapter 5 contains a brief summary and scope for future work.

CHAPTER 2

PROCESS DEVELOPMENT ON ADVANCED THIN MATERIALS, FABRICATION AND TESTING

The Embedded Actives and Passives (EMAP) consortium at the Packaging Research Center at Georgia Tech has been working on low loss ultra-thin substrates so as to come up with a comprehensive solution for mobile products. This program aims to drastically decrease package profile by using thinner materials and embedded actives and passives. The performance benefits that accrue by using this technology make it very attractive. This work aims to explore and demonstrate the use of ultra-thin low loss substrate with high density wiring. A schematic is shown in Figure 2.1.

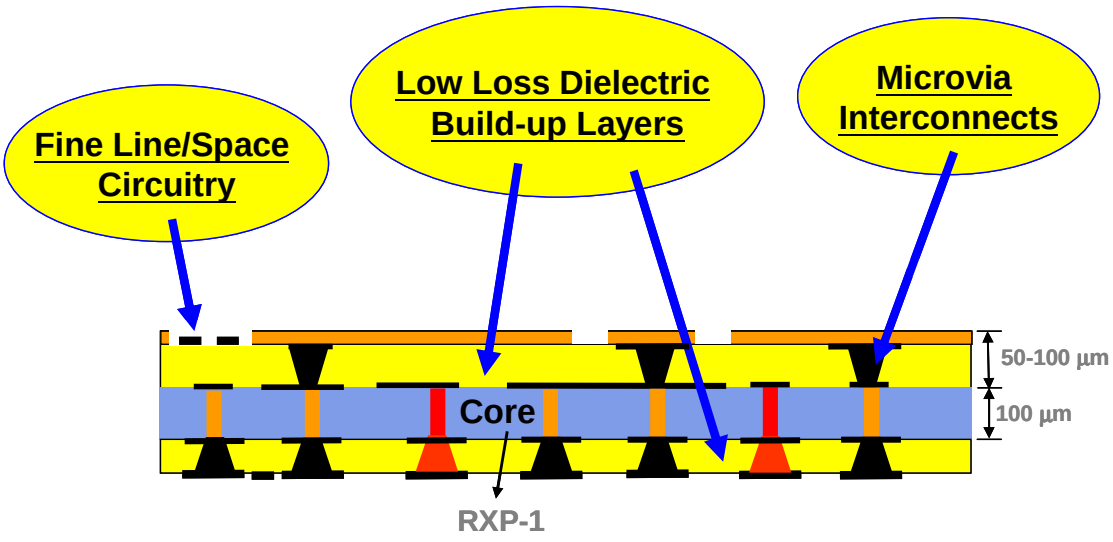


Figure 2.1 Schematic of ultra-thin low-loss substrate with high density wiring

This chapter deals with the process optimizations made on a new advanced material set in order to obtain high wiring density and reliability. The low loss thin film build-up dielectric is called RXP-4 and the low loss core is called RXP-1. The RXP-1 core is a glass fiber reinforced organic laminate with thickness in the range of 50-100µm. RXP-1 has stable dielectric constant of 3.25 and loss tangent of 0.004 at 1-20GHz. The RXP-4 build-up film has stable dielectric constant <3 and loss tangent of 0.0043 at 1-20 GHz, and film thickness of 20µm. First, the optimization of the photolithography process for obtaining fine lines is described. Next, research on the lamination profile of RXP-4 and via ablation is presented. Finally, the entire process flow used to fabricate two test vehicles, one to study via reliability and the other to study warpage and demonstrate assembly. Testing methods are finally described.

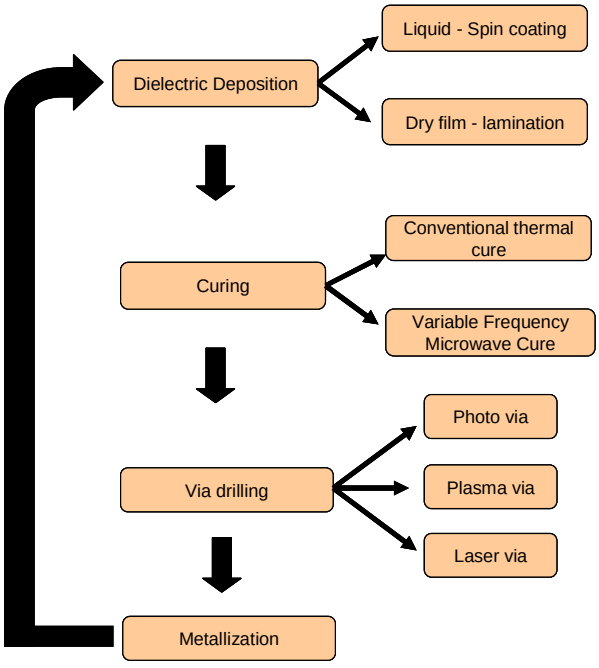


Figure 2.2 Process flow for fabrication of multi-layer high density substrate

2.1. Typical Fabrication Process Flow for High Density Substrates

Fabrication of high density circuits is typically accomplished by depositing alternate layers of dielectric and conductor. Figure 2.2 shows the typical process flow for fabrication of such a substrate.

In general, a core substrate consisting of a reinforced dielectric with a laminated copper foil is patterned first. This is accomplished by the so called subtractive metallization process which will be described below. Once the core is metalized, the next layer of dielectric is deposited and the metallization performed by semi-additive plating while ensuring accurate alignment.

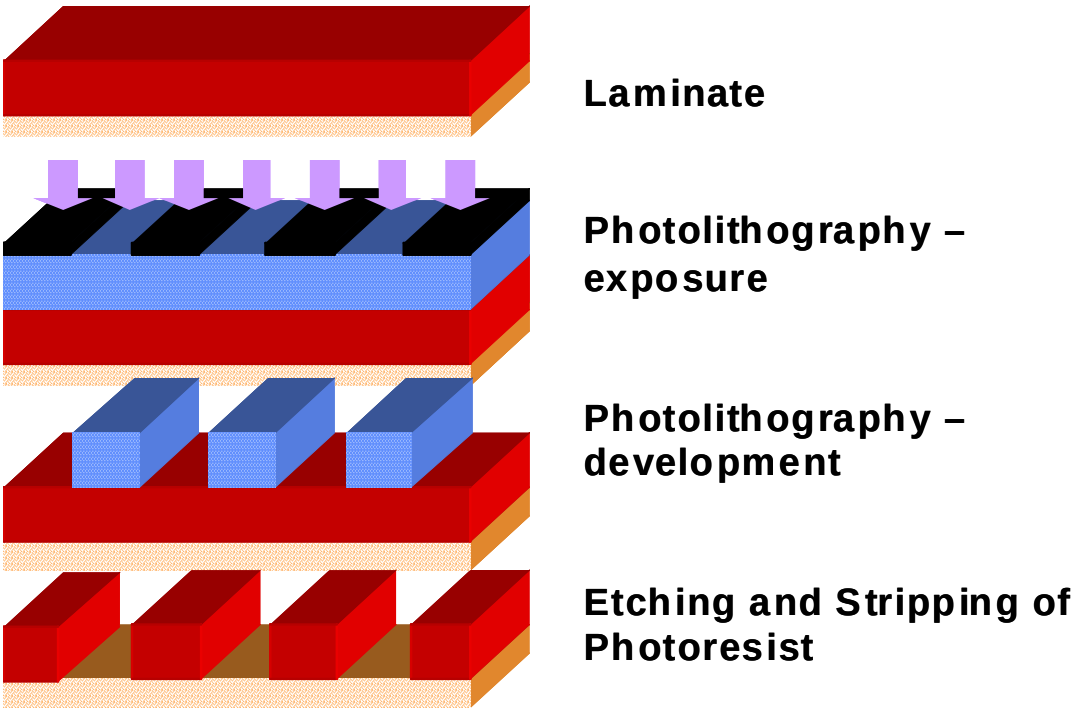


Figure 2.3 Subtractive metallization of dielectrics

As mentioned previously, there are two primary methods of circuit formation – subtractive and semi-additive. Subtractive processing (Figure 2.3) uses a copper clad dielectric and subtracts the unnecessary pattern of copper from the surface by chemical etching, leaving the copper traces. Photolithography is used to control the areas to be etched. Photoresist is deposited on the entire surface of copper and exposed to make the required pattern. After development, only those areas where copper needs to stay will have photoresist.

These areas will be protected during the etching process by the photoresist layer. The main advantage of the subtractive process is the excellent adhesion of the copper foil to the substrate. Limitations of the subtractive etching process stem from the isotropic nature of the etching process. This results in undercut of the line and reduces the resolution of the line that can be attained. To attain finer resolution, the thickness of the copper cladding should be reduced. However there is a practical limitation to how thin a cladding can be used.

To overcome the disadvantages of subtractive etching, the semi-additive plating process was designed. Figure 2.4 shows a process schematic of semi-additive plating. A very thin seed layer of copper is plated on the dielectric using electroless plating or sputtering. The function of the seed layer is to provide an electrically conductive surface for the higher throughput electroplating process. The seed layer is then patterned using photolithography and electroplating is performed to generate the required pattern. The photoresist is then stripped and the seed layer etched away. This will of course result in

removal of copper from the patterned areas too. So this should be taken into account while designing the process.

The thickness of the seed layer determines how fine the resolution can be. The thinner the seed layer, the smaller the line and space resolution that can be achieved. This is due to the inherently isotropic nature of wet etching. As the copper gets etched down, etching of the side walls also takes place leading to the formation of trapezoidal lines.

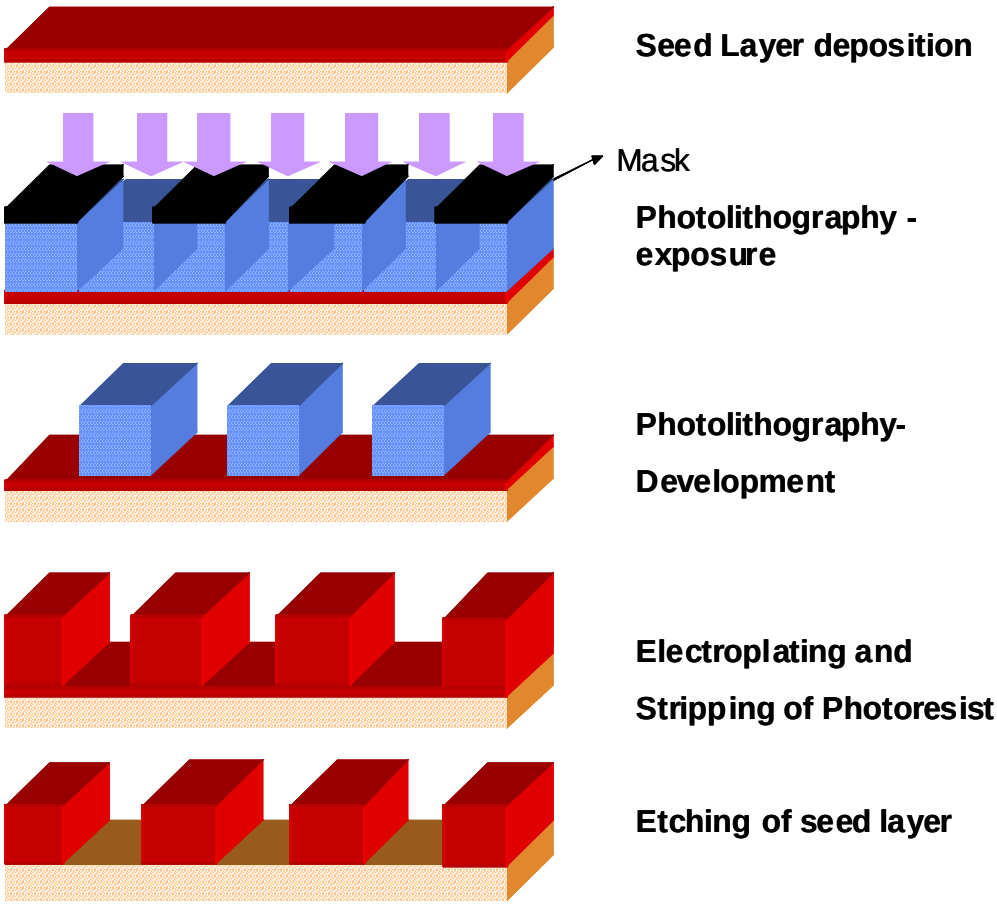


Figure 2.4 Semi-additive metallization of dielectrics

2.2. Development of Advanced Processes for Ultra-thin SOP

2.2.1. Optimization of photolithography process

The exposure and development time during the photolithography process are critical parameters for fabricating ultra high density packages. The photoresist used for fabrication is Riston JSF-1C15. The exposure and development time were carefully optimized in order to get high resolution line and space structures. Line widths down to 15µm were consistently obtained. Figure 2.5 shows 15µm line and space both on RXP-1 (subtractive processing) and RXP-4 (semi-additive processing)

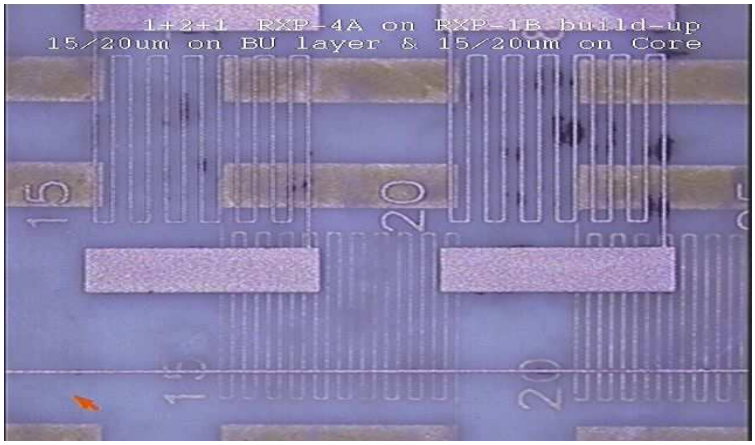


Figure 2.5 15µm line and space on RXP-1 (seen below) and RXP-4 (seen above)

2.2.2. Optimization of lamination profile of RXP-4

RXP-4 is a build-up thin film dielectric that is laminated onto the substrate. The lamination profile used is very critical in order to prevent delamination and to obtain good curing. Based on a number of trials, it was found that hot roll lamination did not produce any adhesion to RXP-1. It was then decided to switch to hot press lamination.

Initial trials using the hot press were found to yield poor results. While the material was found to adhere to the substrate, a number of lamination defects were found. These defects were mostly found to be bubbles or areas where adhesion was poor. Figure 2.6 shows some of these defects.

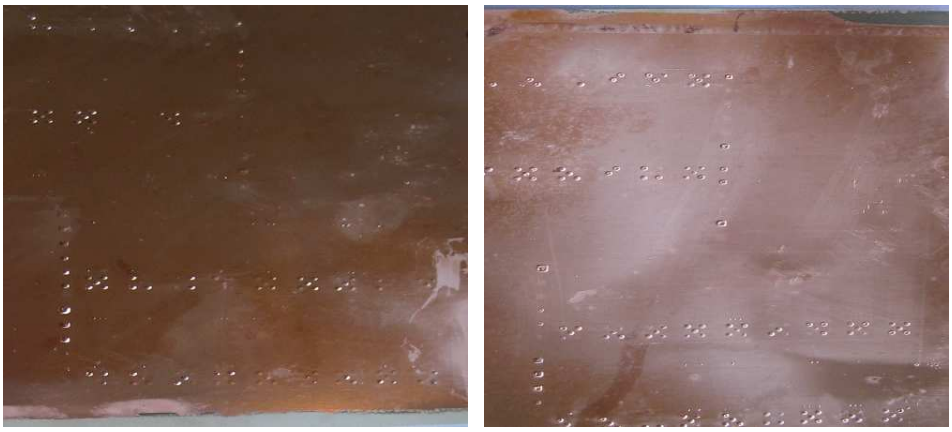


Figure 2.6 Lamination defects on RXP-4

Based on DSC curing studies, it was decided that a higher temperature was required to improve lamination. With this change to the press profile, the visual appearance after lamination was very good, the material was unable to survive chemical roughening treatment which is required for electroless plating of the seed layer. Figure 2.7 shows the improvement achieved in lamination.

Figure 2.7 Improved lamination after process enhancement

The temperature was further increased to prevent problems during electroless plating. With this increase in temperature, most problems were solved. However, blisters were found to appear during electroless plating. In order to solve this problem, the actual surface temperature of the substrate was measured using a thermocouple. It was found that the actual sample temperature lags the machine reading. To compensate for this, the lamination cycle time was increased. This lamination profile was found to impart excellent adhesion and high degree of cure to the dielectric. Figure 2.8(a) shows blistering of the dielectric before process improvements. Figure 2.8(b) shows a dramatic improvement in sample quality after process improvements.

Figure 2.8 (a) Blistering during electroless plating (b) Process improvements lead to defect free plating

The final lamination profile after extensive optimization was found to yield good peel strength values.

2.2.3. Optimization of via ablation processes and plating processes

Microvia ablation was performed using a Nd-YAG laser operating at UV wavelength of 355nm. Optimized plating processes were developed for via diameters in the 25-50µm range. Figure 2.9 shows a 35µm blind via on RXP-4.

Figure 2.9 35µm blind via on RXP-4

2.3. Fabrication of test vehicles (TV)

The optimized processes were used to fabricate two different TVs. One TV contained sub-15µm line and space and sub-50µm vias. The aim of this TV was to demonstrate high wiring density and reliability on thin substrates using next-generation materials. The other TV was used to demonstrate assembly and study the effect of thin substrates on warpage.

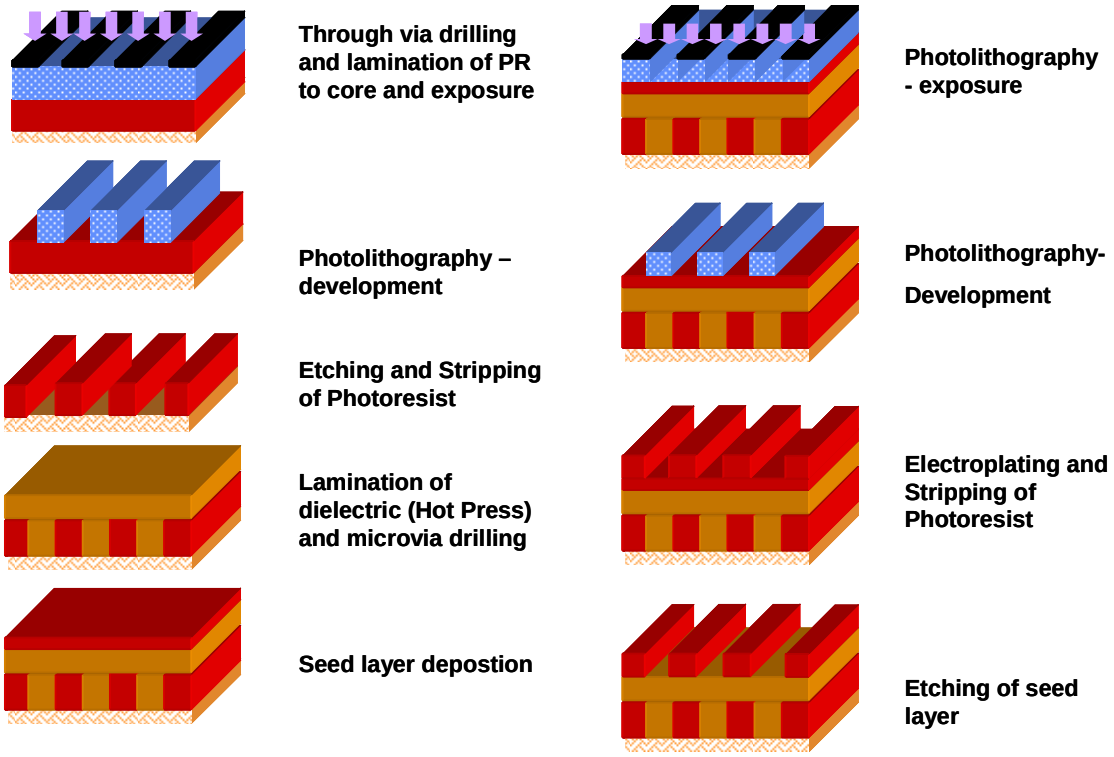


Figure 2.10 Process flow used for fabricating TV (Shows one sided build-up. Both sides were built-up to fabricate TV)

Figure 2.10 shows the process flow used for fabricating the TV. First, RXP-1 core laminate (100µm thickness) was patterned using subtractive etching process. Riston JSF-

1C15 photoresist was laminated using a hot roll laminator. The lamination temperature was 100°C. After ensuring defect free lamination, the photoresist was exposed using a UV exposure tool. The optimized exposure time was used and the photoresist was then developed using a solution of 1% Na_2CO_3. The core laminate was then carefully etched to obtain a pattern.

RXP-4 (25µm) was then laminated on the core using the optimized lamination profile. Vias were then drilled by UV laser. Electroless seed plating was then performed. After ensuring good adhesion of the electroless copper to the dielectric surface, photolithography was again performed. Pattern plating was then done to build up the required thickness of copper.

2.4. Testing

Microvia test vehicles were subjected to MSL-3 preconditioning according to JEDEC/IPC JSTD020D-01. The samples were first baked at 125°C for 24 hours to remove moisture. They were then subjected to a moisture soak using the accelerated condition of 60°C/60% RH for 40 hours after which the samples were passed thrice through solder reflow with a peak temperature of 260°C. The resistance of the daisy chains was then measured to establish a baseline for further testing.

The test vehicles were then subjected to thermal shock testing at -55°C and 125°C in an air-to-air thermal shock chamber according to JESD22-A104C. Electrical continuity of the daisy chains was checked every 200 thermal cycles for assessing the reliability.

2.5. Summary

Fabrication steps which essentially included sequential build-up processes were described with the help of process schematics. The common steps included were lamination, dielectric curing, photolithography, metal etching, electroless plating, electroplating etc. Dimensions and geometry were also described along with details of the processes. The optimization of various processes was described. These optimized processes were used to build an ultra-thin low-loss package substrate consisting of 4 layers with 25µm microvias and 50µm micro through holes. Finally, the testing procedures followed for establishing reliability of these substrates were explained.

CHAPTER 3

FINITE ELEMENT ANALYSIS

Finite element models were developed to study the effect of geometrical parameters and material properties on thin substrate reliability. This chapter discusses the model geometries, material models, boundary conditions and loads and the parameters extracted in post-processing. Two FE models were developed to study different aspects of the challenges involved in thin substrate processing. The first model studied the reliability of microvias and the effect of material properties on the reliability. The second model was developed to address the warpage challenge and to get an estimate of the warpage induced during reflow. The results of the FE analysis are presented together with the experimental results in the next chapter.

3.1. Material Properties and Their Effect on Reliability

Electronic packages are subjected to accelerated thermal cycling as part of qualification to simulate the real time loading that they will undergo. A typical electronic package consists of multiple layers of conductor, typically copper and dielectric. The mismatch in the coefficient of thermal expansion (CTE), results in the differential expansion and contraction of the package during thermal cycling. This differential expansion and contraction induces thermo-mechanical stresses and strains in the package. These strains depend on the global and local CTE mismatch [17]. The modulus of the material also plays a significant role in determining the stresses induced. A stiffer material will experience lesser strain but higher stress as it will not be able to release the

stress by deformation. The geometry of the package is also a determining factor [18, 19]. Based on the particular geometry and the material set, each package will have a distinct thermo-mechanical stress profile. The aim of FE modeling in this work is to understand the factors that could cause failure and to aid in material selection.

3.2. Candidate Materials for Study

As mentioned previously, material properties play an important part in thermo-mechanical reliability. In order to better understand some of the factors that affect reliability in ultra-thin substrates, two different material sets were chosen. The first material set consisted of Bismaleimide triazine (BT) core and Ajinomoto Build-up Film (ABF). The second material set consisted of RXP-1 core and RXP-4 build up film. A brief comparison of the properties of these materials is shown in Table 3.1.

Table 3.1 Properties of candidate materials [20]

Material	Diel. Cons.	Loss Tgt.	Elastic Modulus	CTE	Elongation to Break (%)
Build-up Dielectric					
RXP-4	2.95	0.0043	2.1 GPa	67 ppm/°C	9
ABF GX-13	3.3	0.012	4.8 GPa	46 ppm/°C	5
Reinforced Dielectric					
RXP-1	3.48	0.0037	9-11 GPa	12 ppm/°C	2.3
BT	4.6	0.008	17 GPa	14 ppm/°C	N/A

It can be seen from Table 3.1 that RXP-4 has extremely low loss (0.0043). This is required for leading edge high frequency applications. RXP-1 similarly has very low loss

(0.0037). While the CTE of RXP-4 is slightly higher than ABF, the lower modulus is expected to compensate for this. With RXP-1, the lower modulus and CTE as compared to BT should aid in increased thermo-mechanical reliability.

ABF is known to have low elongation to failure of 5%. This causes cracking of the dielectric when laminated on thin cores which have low stiffness. RXP-4 with its higher elongation to failure is expected to perform better when integrated with thin cores.

3.3. Material Models

Material models are the most important aspect of FE analysis. To obtain accurate results, it is essential that accurate material models are utilized. Typically, material properties vary with temperature. In general, most FE analyses utilize a single number for a given material property for the entire range of analysis. This work attempts to include the temperature dependent nature of material properties. Young's modulus and CTE for a material are input into the model as a function of temperature.

Table 3.2 lists the various material models that were employed.

Table 3.2 Material Models

Material	**Model**
BT	Temperature Dependent Linear Elastic with Orthotropic CTE
RXP-1	Temperature Dependent Linear Elastic with Orthotropic CTE
ABF	Temperature Dependent Linear Elastic with Orthotropic CTE
RXP-4	Temperature Dependent Linear Elastic with Orthotropic CTE
Copper	Bilinear Elastic-Plastic
Silicon	Linear Elastic
Solder(95.5Sn/3.8Ag/0.7 Cu)	Anand Visco-Plastic

Figure 3.1 and Figure 3.2 illustrate the CTE of the core and build-up materials against temperature. As can be seen, RXP-1 has an optimal CTE of 10-12 ppm/°C almost throughout. On the other hand, RXP-4 displays a dramatic increase in CTE after 125°C or so. This is expected to be compensated by the lower modulus of RXP-4 which allows it to be more conformal and absorb more stress. The modulus of the materials is shown in Figure 3.3 and Figure 3.4.

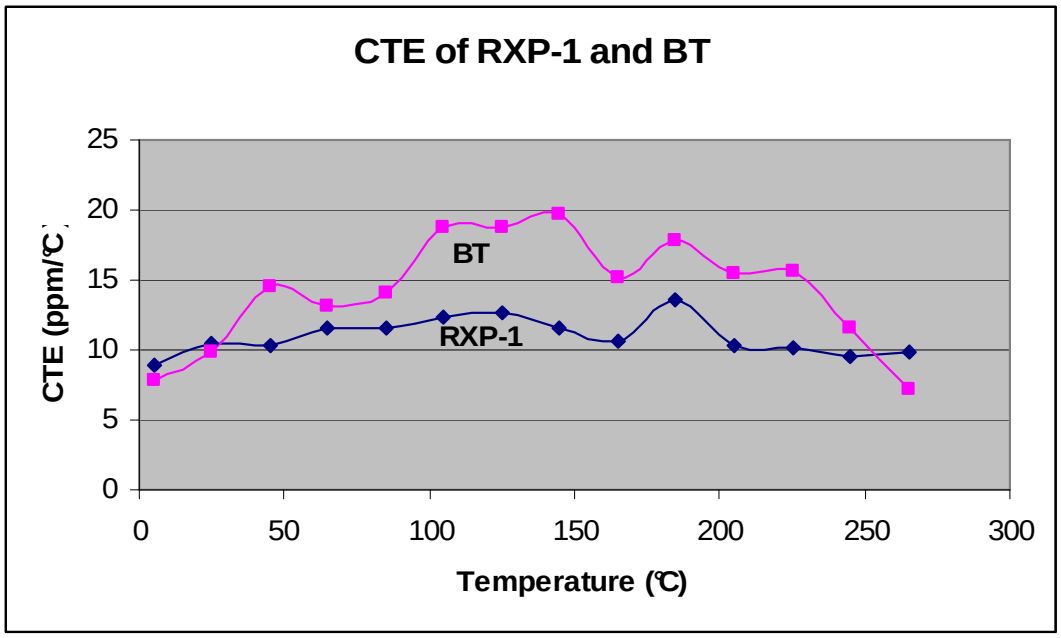


Figure 3.1 CTE comparison of BT and RXP-1

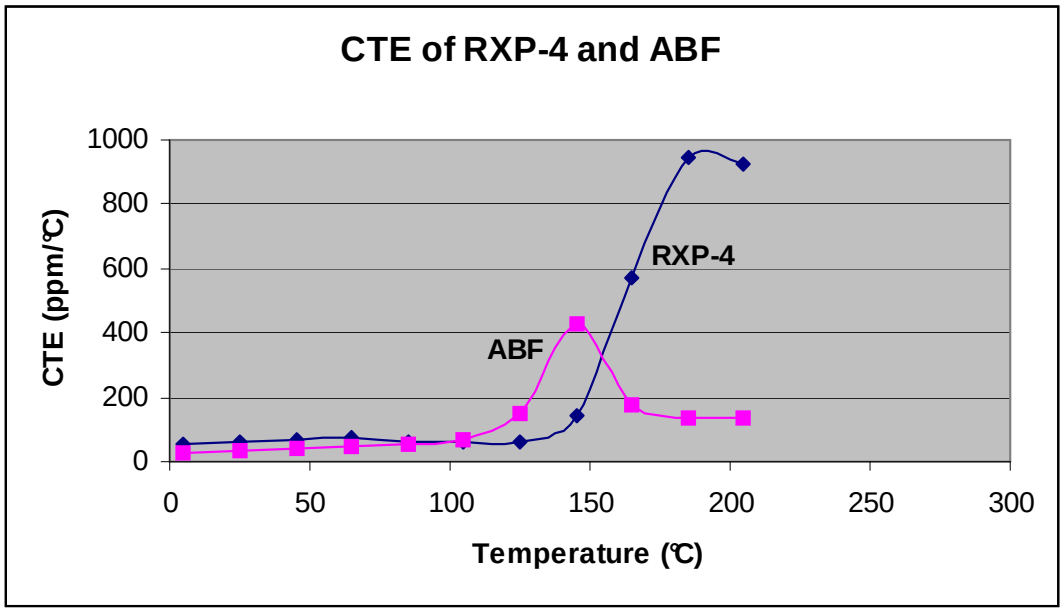


Figure 3.2 CTE comparison of ABF and RXP-4

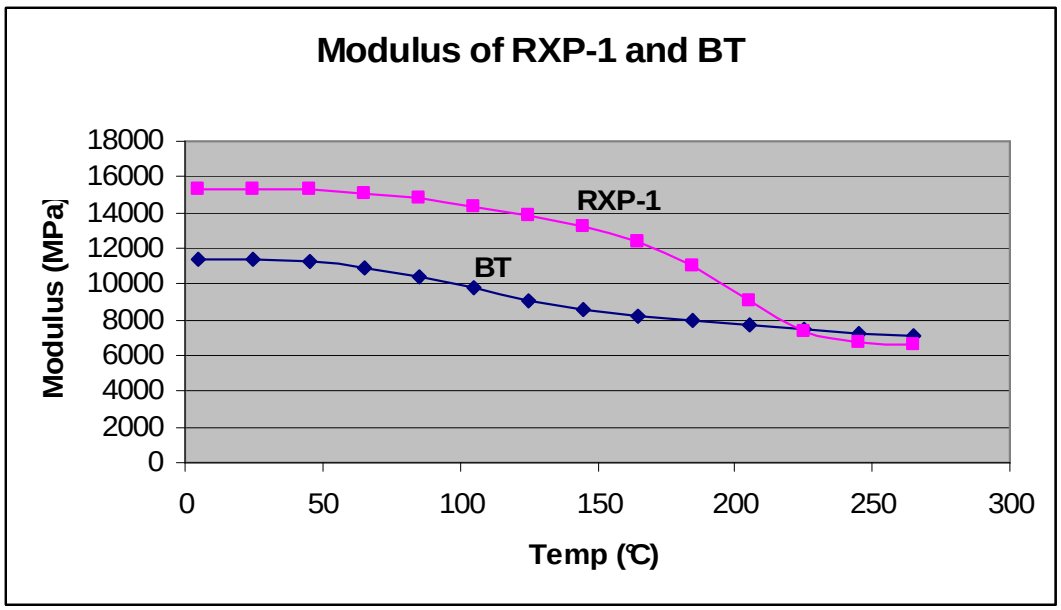


Figure 3.3 Modulus comparison of BT and RXP-1

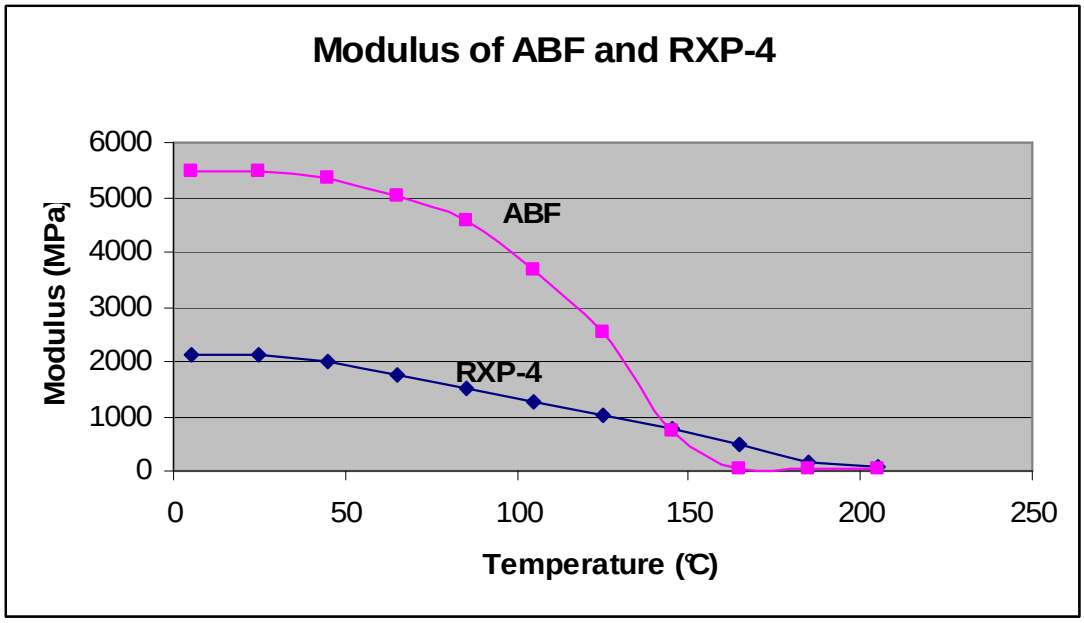


Figure 3.4 Modulus comparison of ABF and RXP-4

3.4. Geometry Modeling

The FE analysis was performed using ANSYS®. The geometry was built in a fully parametric fashion for both the microvia and warpage models. The geometry, loading conditions and parameters used for both models are discussed below.

3.4.1. Model for Microvia Reliability

The geometry used for assessing microvia reliability is shown in Figure 3.5. The dimensions are only indicative as geometric parameters were varied in order to obtain an understanding of their effect on reliability. In view of computation requirements, an axisymmetric model was considered to be sufficiently accurate. The parameters used for this model are listed below:

Thickness of Core Substrate	Thickness of Build-up Copper
Thickness of Dielectric	Diameter of Via
Thickness of Core Copper	Thickness of Via Copper

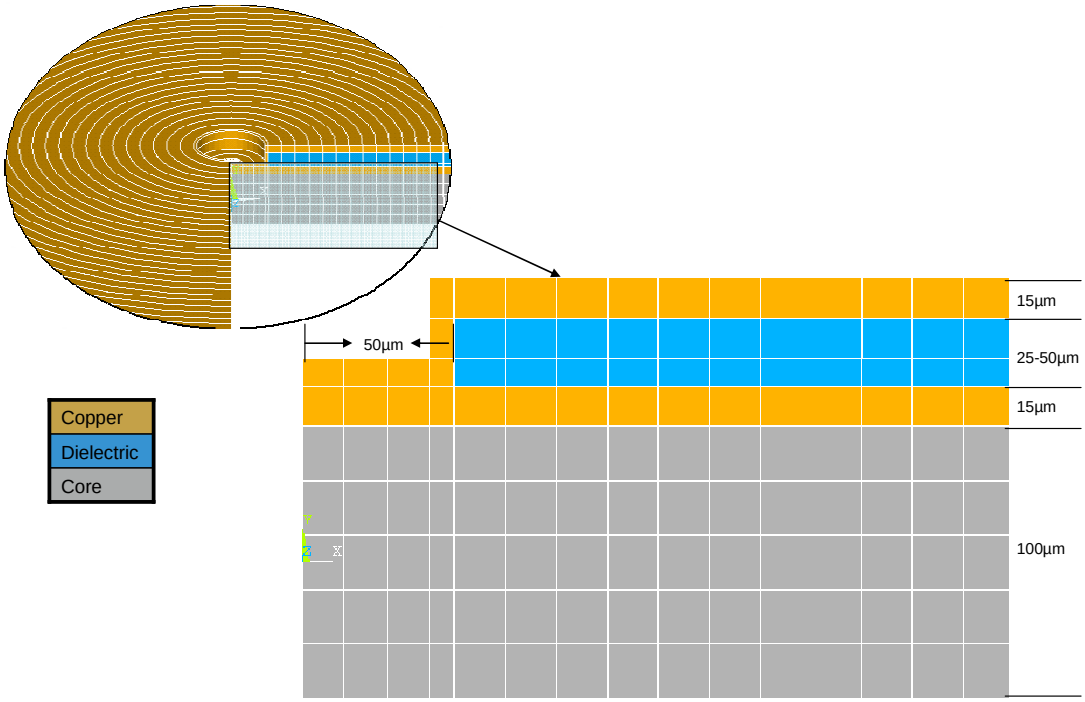


Figure 3.5 Axisymmetric model for microvia reliability

The thermal profile for the simulation consisted of solder reflow, followed by thermal shock cycling between –55°C and 125°C with a 10 minute dwell at the extreme temperatures. The thermal profile is shown in Figure 3.6.

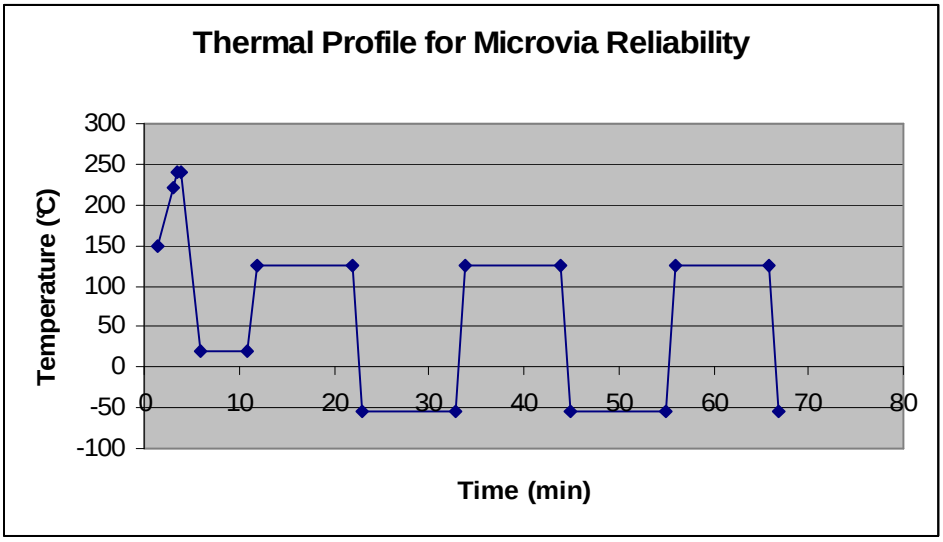


Figure 3.6 Thermal Profile for Microvia Reliability

Figure 3.7 shows the elements that were considered for computing the area average stress and comparing stress values across different material combinations.

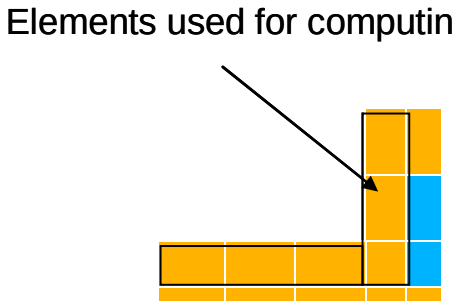


Figure 3.7 Strip of elements used for calculation of area average stress

3.4.2. Model for Warpage Prediction

Previous work in this area has suggested that a stiff core is desirable to reduce warpage [21-23]. This work attempts to understand the effect of a less stiff core on thermo-mechanical reliability.

The geometry of the model is shown in Figure 3.8. The parameters used for the model are listed below:

Thickness of Core Substrate

Thickness of Core Copper

Thickness of Dielectric

Diameter of Solder Ball

Thickness of Silicon Die

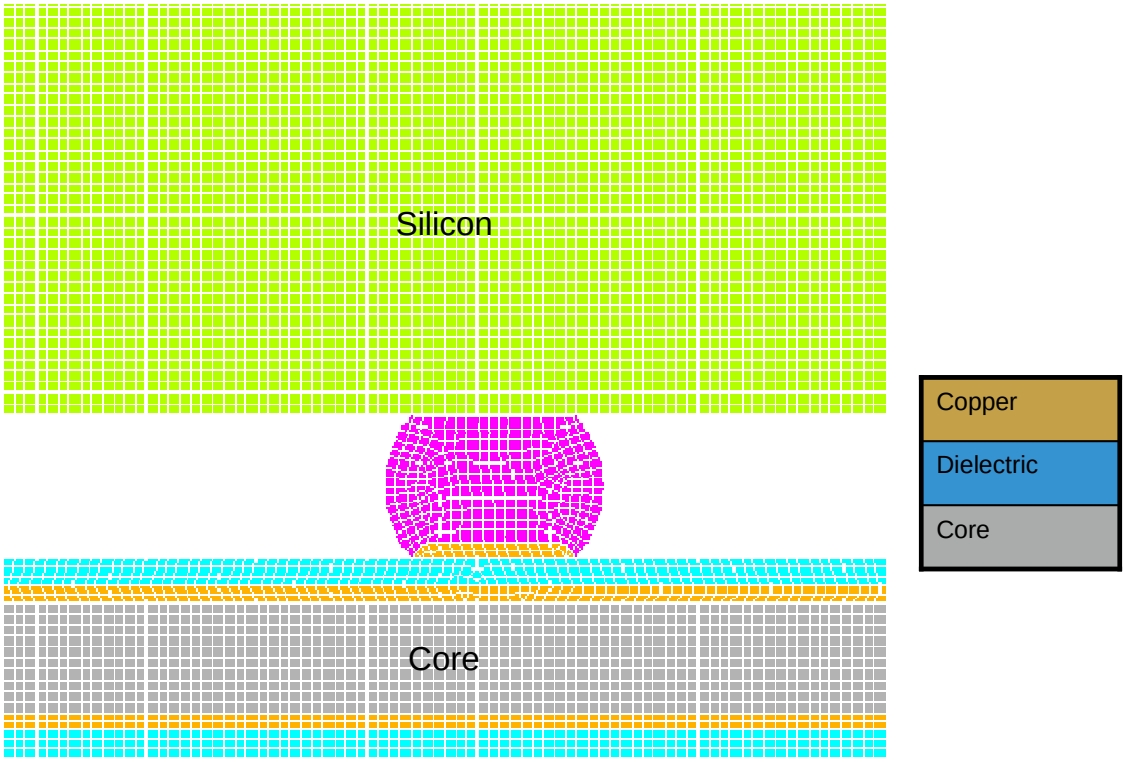


Figure 3.8 Geometry for warpage prediction

The thermal profile used was essentially that of a solder reflow. The warpage was calculated at different point along the cycle. The aim of this simulation was to compare the warpage between a thick substrate and a thin substrate. At the same time, the stresses

in these substrates were compared to understand the effect of a thin substrate on thermo-mechanical reliability.

3.5. Summary

This chapter described the material models, geometry and loading conditions used in the two FE models. The model for assessment of microvia reliability used a temperature cycling test for predicting reliability. The warpage prediction model aimed to provide an understanding of thermo-mechanical reliability in thin substrates. The warpage of thin and thick substrates was compared. The stresses generated within the package were computed and an attempt was made to understand the effect of thin substrates on stresses.

CHAPTER 4

RESULTS AND DISCUSSION

This chapter presents both the experimental and FE results. The results of process optimization have already been presented in Chapter 2. This chapter describes how that process research was utilized to build test vehicles (TV) to evaluate microvia and micro through hole (MTH) reliability and to assess the effect of warpage on assembly. FE analysis was performed to get a better understanding of some of the factors affecting via reliability and warpage. Finally, assembly on this substrates is demonstrated.

The cross-section of the fabricated TV with microvias and MTH is shown in Figure 4.1.

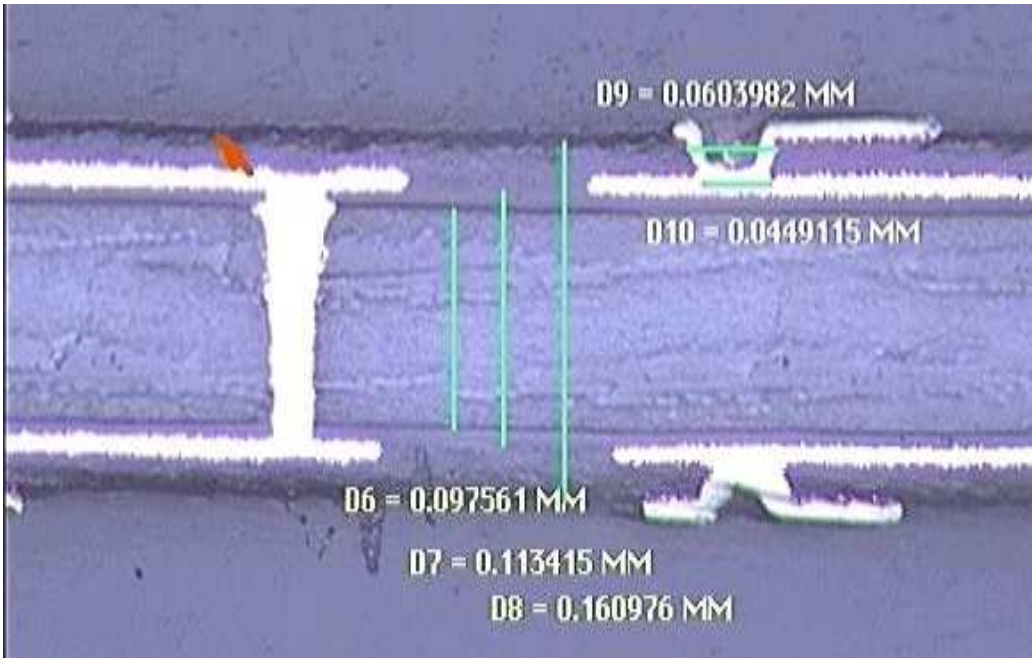


Figure 4.1 Cross-section of fabricated TV

4.1. Microvia and MTH Reliability

The 4 layer ultra-thin test vehicle that was built consisted of three types of daisy chains – microvia daisy chains, micro through hole daisy chains and a daisy chain consisting of both microvias and MTH. The test structure is shown in Figure 4.2.

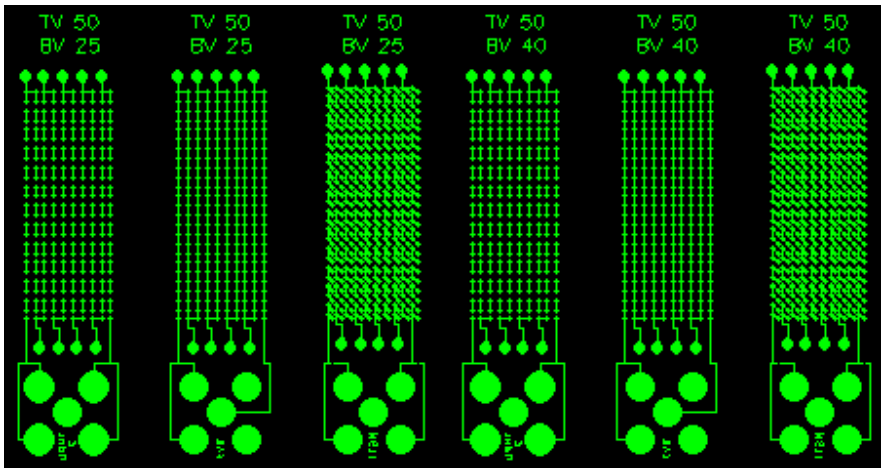


Figure 4.2 Daisy chain test structures consisting of various via diameters

The TV consisted of more than 5000 microvias and MTH. The ultra-thin TV was subjected to thermal shock testing as described in Chapter 2. The vias were found to be reliable and survived for more than 1000 cycles. The yield was found to be 74.8% as fabricated. The blind vias were 50, 40 and 25µm in diameter. The micro-through holes were 50µm in diameter. After 1000 cycles, about 2% of the vias were found to have failed. None of the MTH failed. This shows that the reliability of these substrates is excellent. The results are summarized in Table 4.1.

Table 4.1 Failure rate of microvias

No. of cycles	MTH Diameter (µm)	Microvia Diameter (µm)		
	50	50	40	25
100	0	0	0	0
500	0	2.8%	0.6%	1.6%
600	0	3.8%	0.6%	2.1%
800	0	4.7%	1.2%	2.1%
1000	0	4.7%	1.2%	2.1%

4.2. Fatigue Modeling

FE modeling of the experimentally tested geometry indicated that the total strain range (TSR) was 0.001. This was used to calculate fatigue life using the Engelmaier relation. This non-linear relation can be iteratively solved to determine the mean life to failure (N_f) for a given TSR ($\Delta\varepsilon_r$). One important point that should be noted in this equation is that the number of cycles to failure is a function of the ductility coefficient (ε_f) of copper. The value of ε_f is reported in literature to vary between 0.15-0.3. Therefore, the fatigue life estimate for the microvia is in the form of an upper and lower bound.

$$N_f^{-0.6} \times \varepsilon_f^{0.75} + \frac{0.9}{E}\sigma\left[\frac{e^{\varepsilon_f}}{0.36}\right]^{0.1785\log_{10}\left[\frac{10^5}{N_f}\right]} = \Delta\varepsilon_R \qquad \text{…….(1)}$$

Where N_f is number of cycles to failure

$\Delta\varepsilon_r$ is the total strain range

ε_f is the ductility coefficient of copper (0.15-0.3)

σ is the ultimate tensile strength of copper (260 MPa)

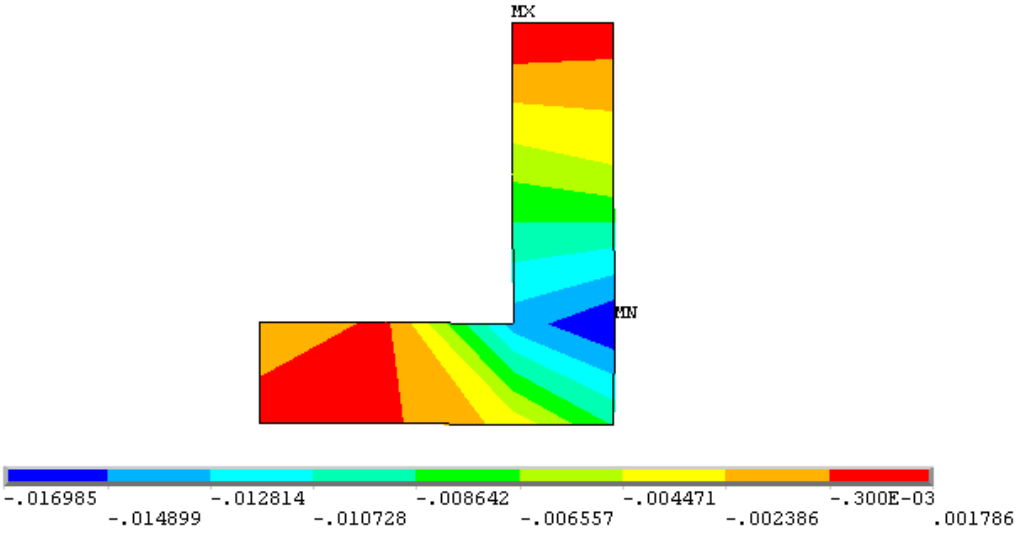
E is the Young's Modulus of copper

Solving the equation resulted in a lifetime prediction of > 10^6 cycles. This is in accordance with experimental testing which shows that the microvias survived > 1000 cycles with almost no failures.

4.3. Comparison of Microvias in ABF/BT and RXP-4/RXP-1 Systems

The ABF/BT and RXP-4/RXP-1 material systems were compared. Via reliability has been demonstrated on ABF [5]. Figure 4.3 shows the Z component of via strains after cycling. Microvias in the RXP-4/RXP-1 system show slightly lower strains than ABF/BT.

ABF/BT



RXP-4/RXP-1

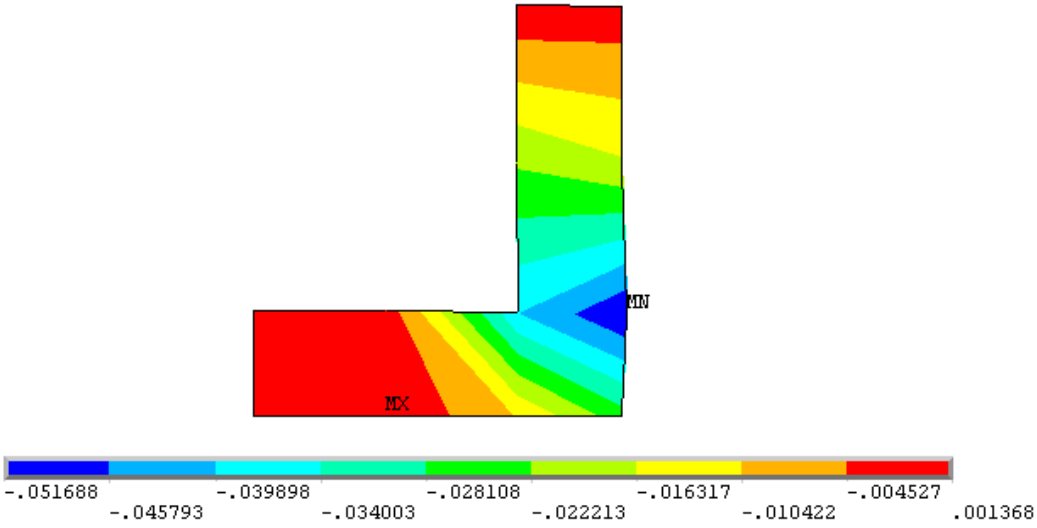


Figure 4.3 Z component of via strains after cycling

Axial stress in the dielectric was also extracted from FE modeling. This was done to compare the chances of dielectric cracking in the case of RXP-1/RXP-4 and BT/ABF which is commonly used. It was found that RXP-4 develops stresses much lower than ABF. This is shown in Figure 4.4.

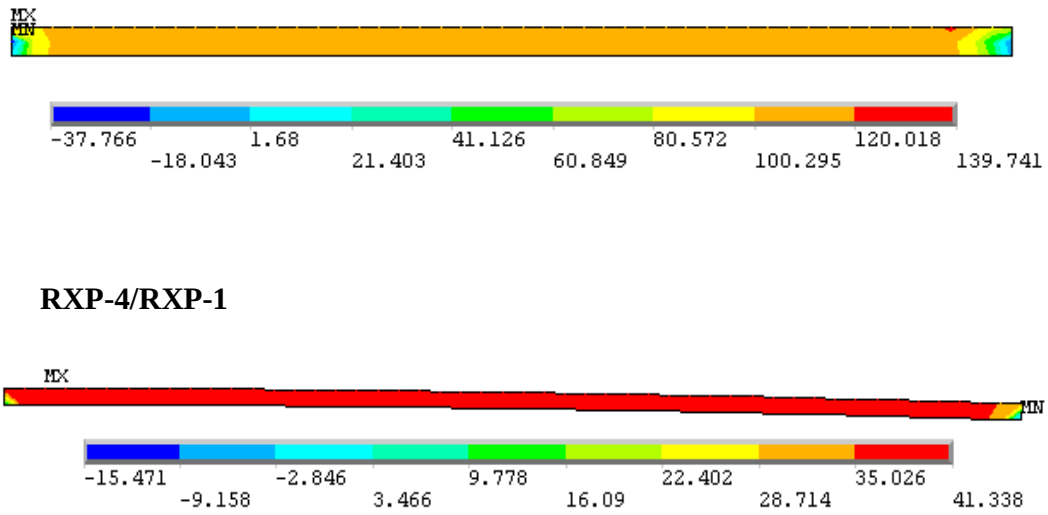


Figure 4.4 Axial stresses in the dielectric after cycling

This shows that both the via and the dielectric are likely to be more reliable in the RXP-4/RXP-1 system. Dielectric cracking is very likely to occur in the ABF/BT system.

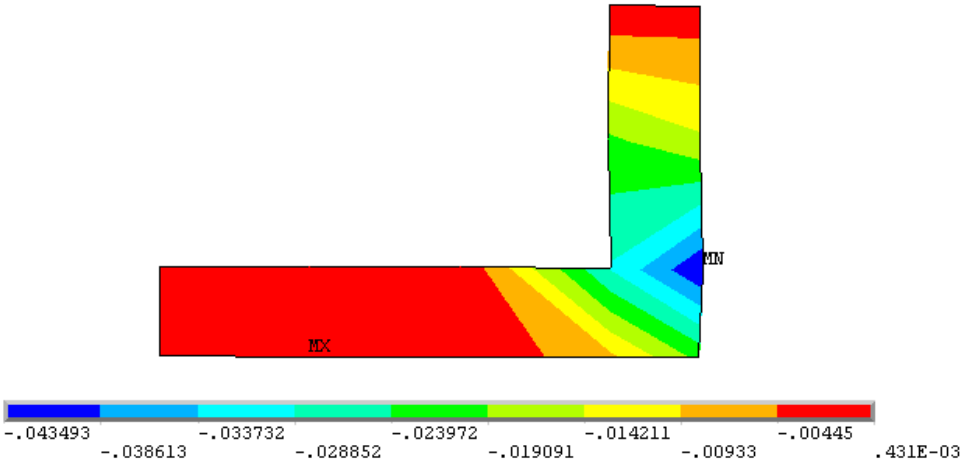
4.4. Effect of Geometry and Material Properties on Microvia Reliability

The effect of various parameters on via reliability is now considered. Geometry and material properties have a profound impact on via reliability.

4.4.1. Effect of Via Diameter

Decreasing the diameter of the via is found to cause an increase in via strains. This is in accordance with previous work [13]. A comparison of the via strains with diameter is shown in Figure 4.5. This comparison was made on the basis of 25µm dielectric. It can be seen that the strain increases slightly until the aspect ratio of the microvia is 1:1. When the depth of the via exceeds the diameter of the via, there is a drastic increase in via strains. This can be attributed to the increased stress concentration in the via due to the low aspect ratio.

100 µm



50 µm

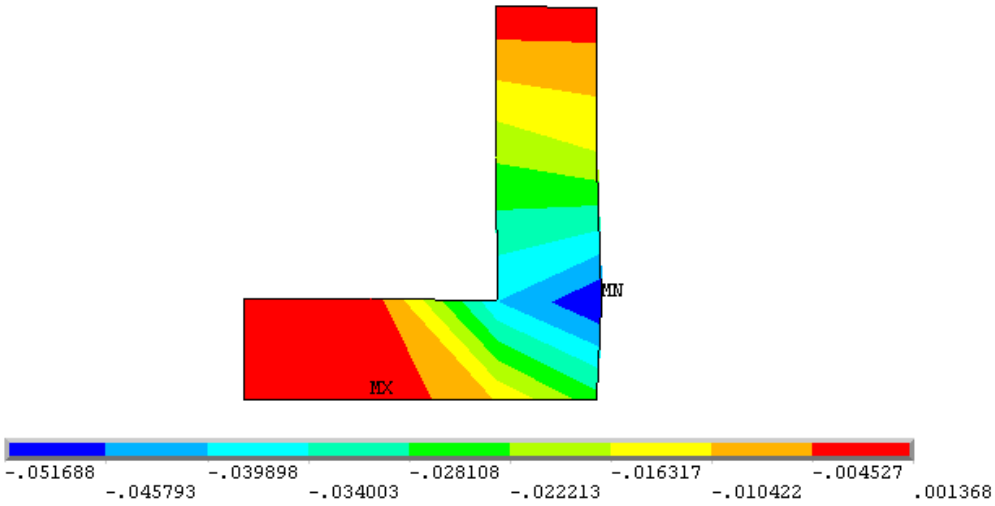
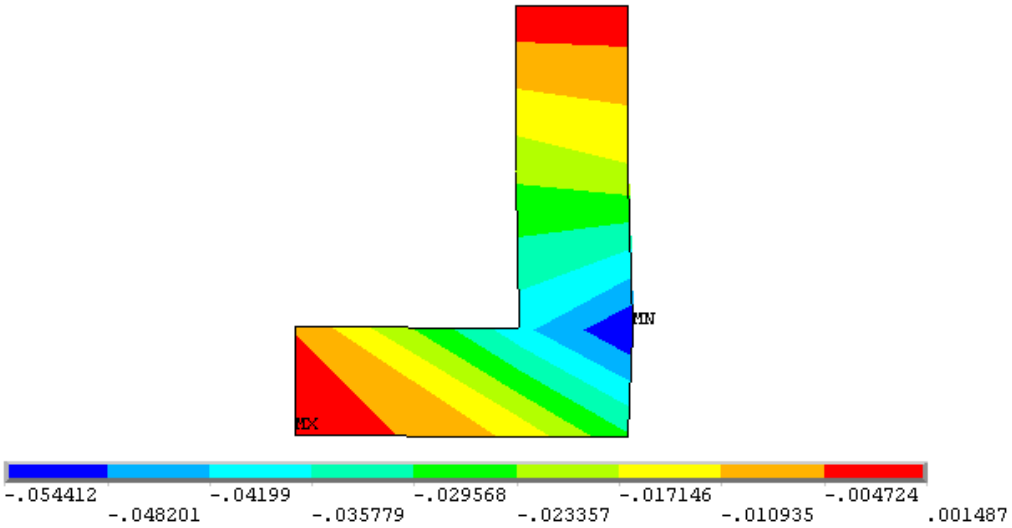


Figure 4.5 Variation of strain in microvias with diameter

40 µm



25 µm

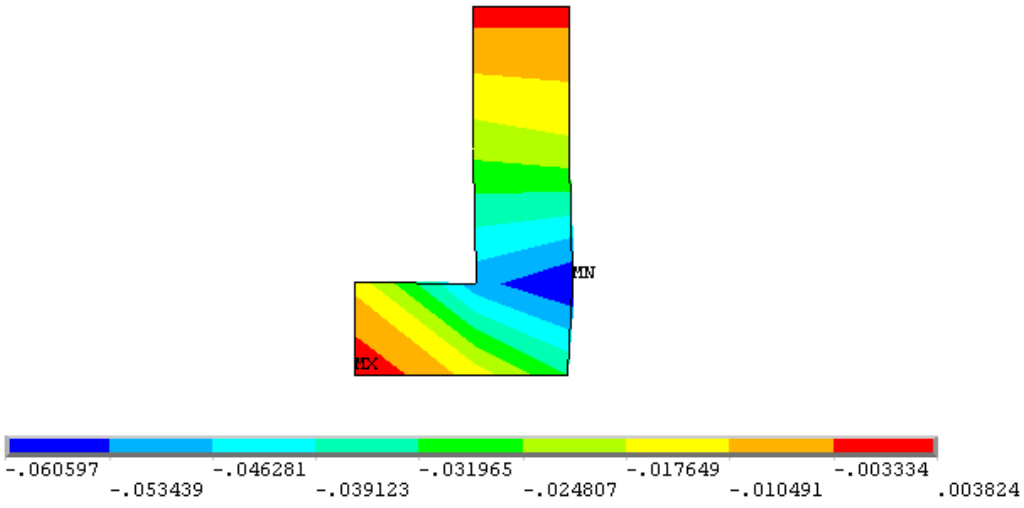


Figure 4.5 Continued

10 µm

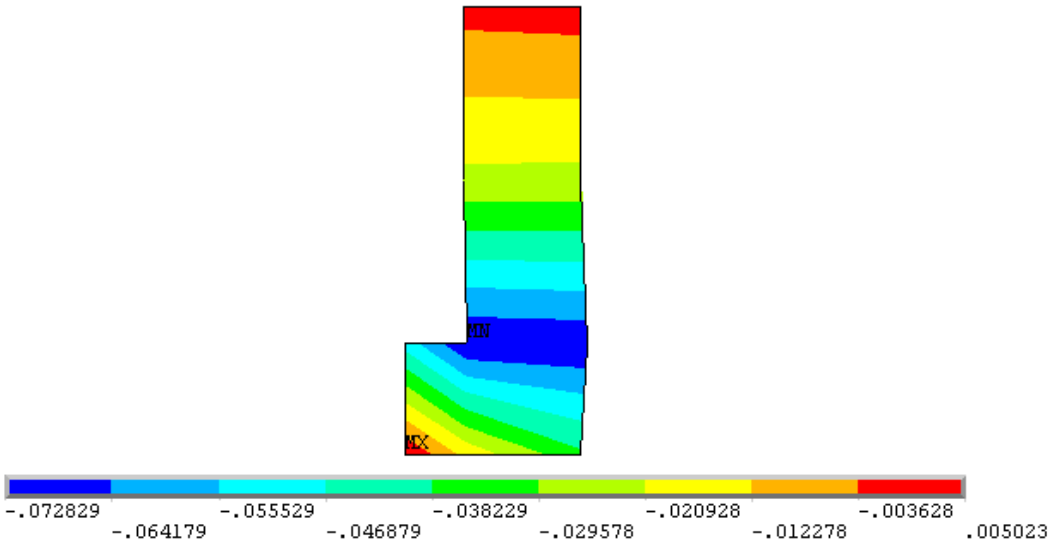


Figure 4.5 Continued

The TSR for different diameters were computed. The results are summarized in Table 4.2. It can be seen that the lifetime decreases dramatically for the 10µm via.

Table 4.2 Variation of TSR and fatigue life with via diameter

Diameter (µm)	TSR	Lifetime Prediction
100	.0013	$1.6x10^7$ cycles
50	.001428	$9.1x10^7$ cycles
40	.001423	$9.4x10^7$ cycles
25	.001511	$5.1x10^7$ cycles
10	.00652	1243

4.4.2. Effect of Material Properties

FE modeling indicated that at these low thicknesses the core has a very minor effect on via reliability. Figure 4.6 shows that the variation in strain of the microvia with increase in elastic modulus of the core. Variation in core thickness was also found to have a minor effect on via reliability. This is shown in Figure 4.7. Since the via is far from the core, the local CTE mismatch is more important.

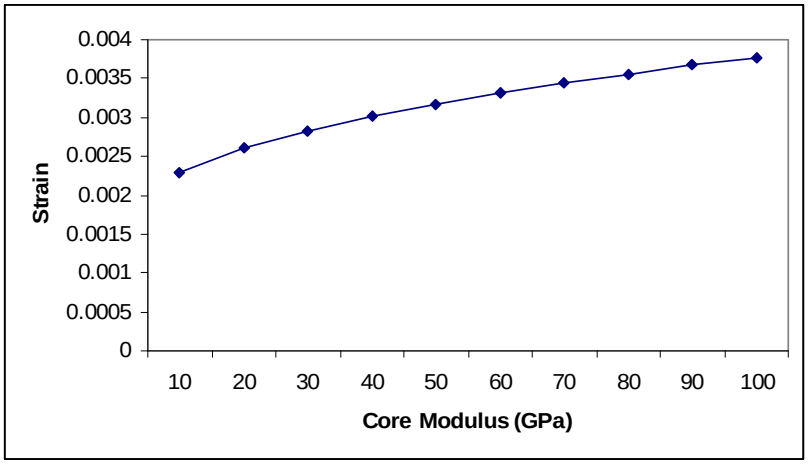


Figure 4.6 Effect of core elastic modulus on microvia reliability

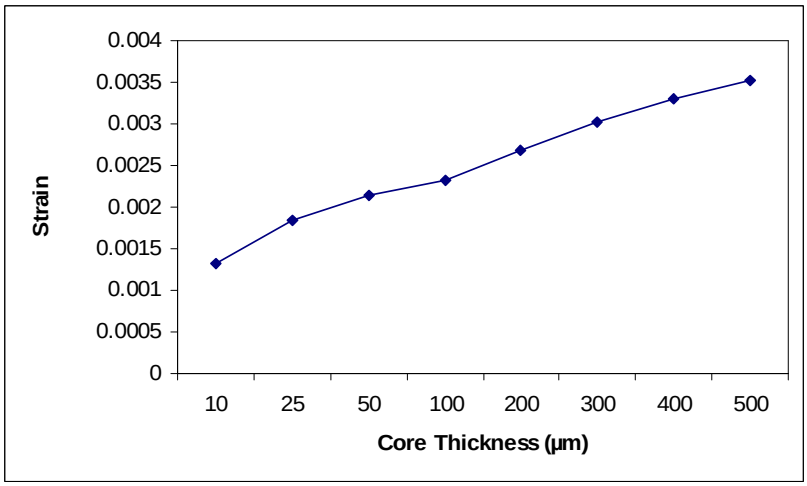


Figure 4.7 Effect of core thickness on microvia reliability

Thus, the properties of the dielectric are the most significant factor in via reliability. This is in accordance with previous results obtained by others [13, 22].

Based on FE modeling, it was confirmed that the design guidelines previously elucidated [13] still apply to thin substrates.

4.5. Warpage of Thin Substrates

Warpage was extracted from FE simulations for a thick substrate with ABF build-up and BT core. This was compared with a thin substrate comprising RXP-4 and RXP-1. The warpage was also extracted for ABF on 100µm BT. As expected, the warpage values were substantially lower for the thicker substrate. The warpage values obtained at different points in the solder reflow cycle are shown in Table 4.3. The warpage of thin ABF/BT and RXP-4/RXP-1 substrates is quite similar. However, ABF/BT has lower warpage at a higher temperature which would be advantageous in assembly.

Table 4.3 Warpage during solder reflow

Material / Temp.	ABF (25µm)/ BT(500µm)	ABF (25µm)/ BT(100µm)	RXP-4 (25µm)/ RXP-1 (100µm)
150°C	6.62µm	30.5µm	27.8µm
240°C	3.75µm	27.2µm	42.5µm

The warpage of the RXP-4/RXP-1 system was also measured using Shadow Moiré [24]. While the values were not found to match in magnitude, the trends were found to be the same. The warpage was found to increase with an increase in

temperature. This is shown in Figure 4.8 and Figure 4.9. The warpage is found to increase from around 26 mils to 31 mils with the increase in temperature from 150°C to 240°C. This can be compared to the increase in warpage from around 28 µm to 43 µm that is predicted by FE modeling. The mismatch can be attributed to the warpage induced by handling and processing.

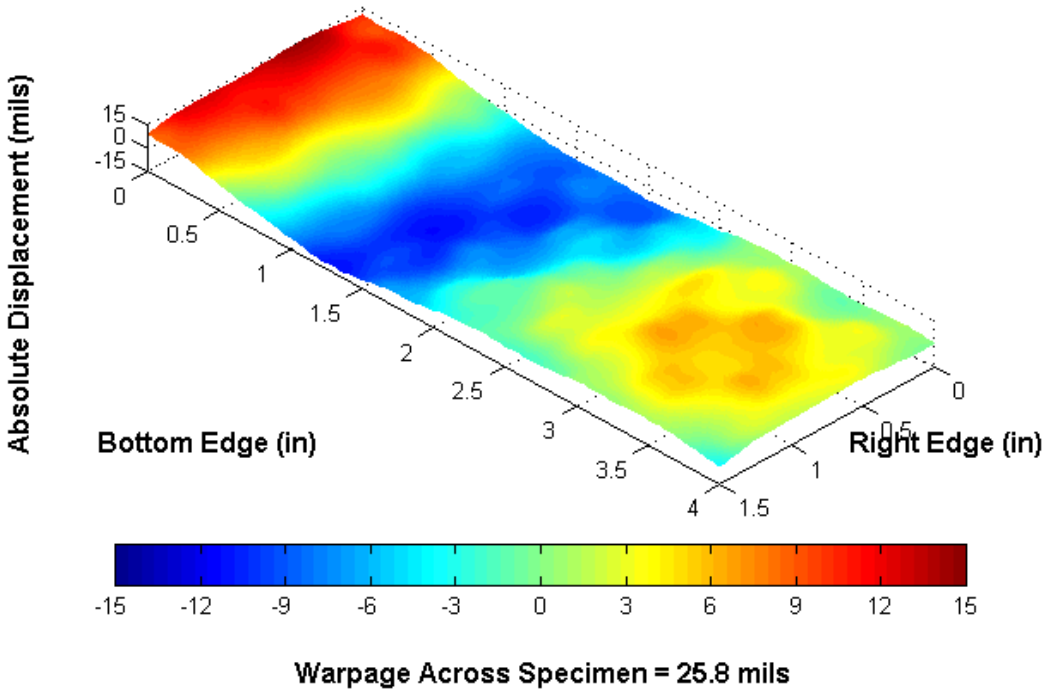


Figure 4.8 Warpage plot of RXP-4/RXP-1 at 150°C

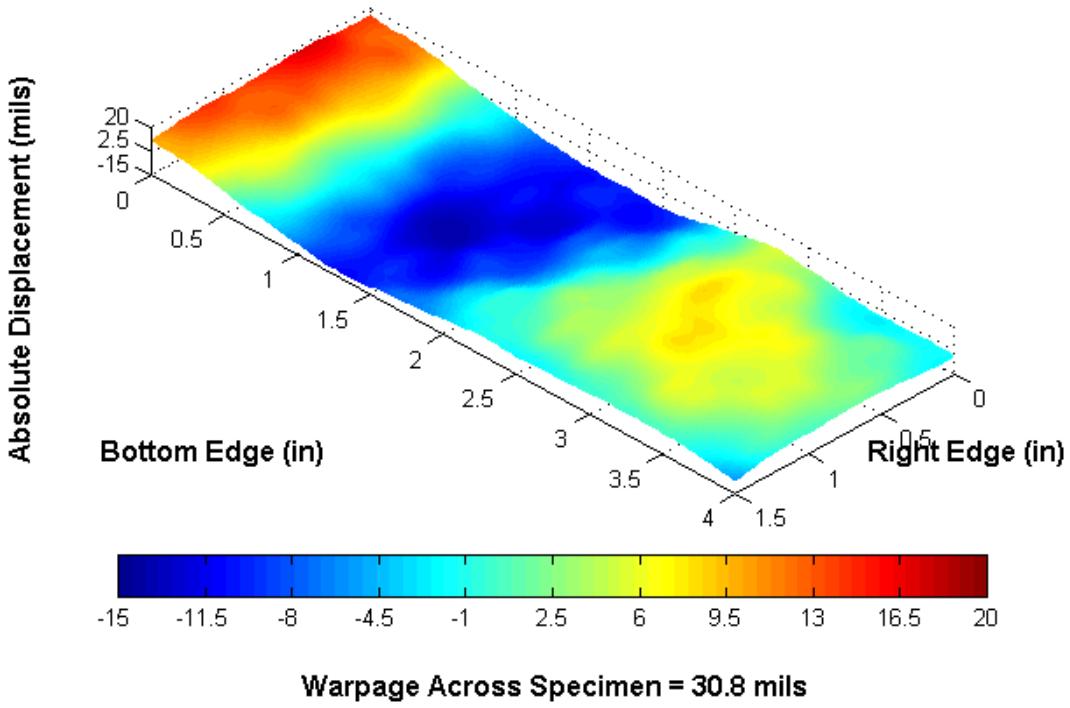
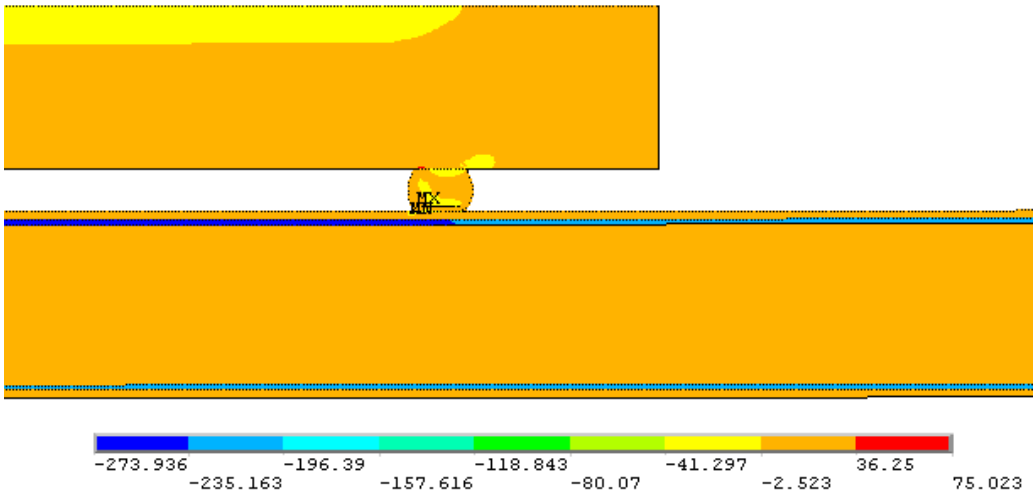


Figure 4.9 Warpage plot of RXP-4/RXP-1 at 240°C

The effective stresses (Von Mises stress) induced in the die and the substrate were compared in the ABF/BT and RXP-4/RXP-1 system. The stress at 150°C is found to be lower in the RXP-4/RXP-1 system (Figure 4.10). However, at 240°C, the RXP-4/RXP-1 system has slightly higher stress as compared to the ABF/BT system (Figure 4.11).

ABF/BT



RXP-4/RXP-1

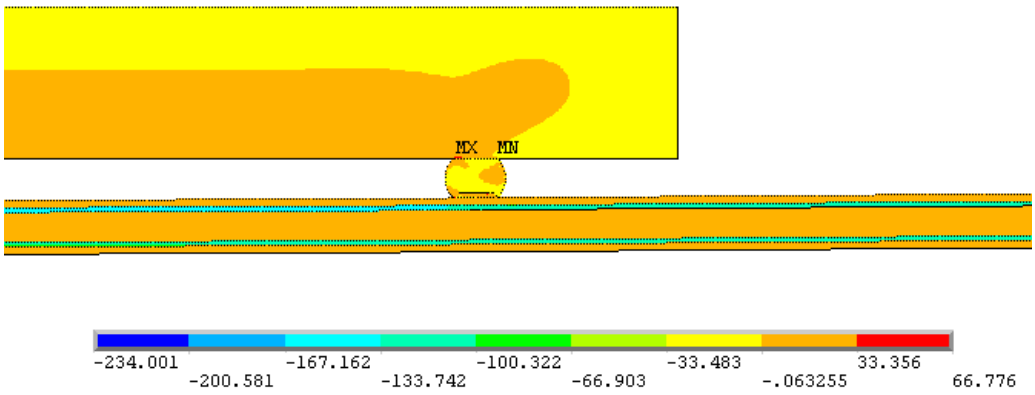
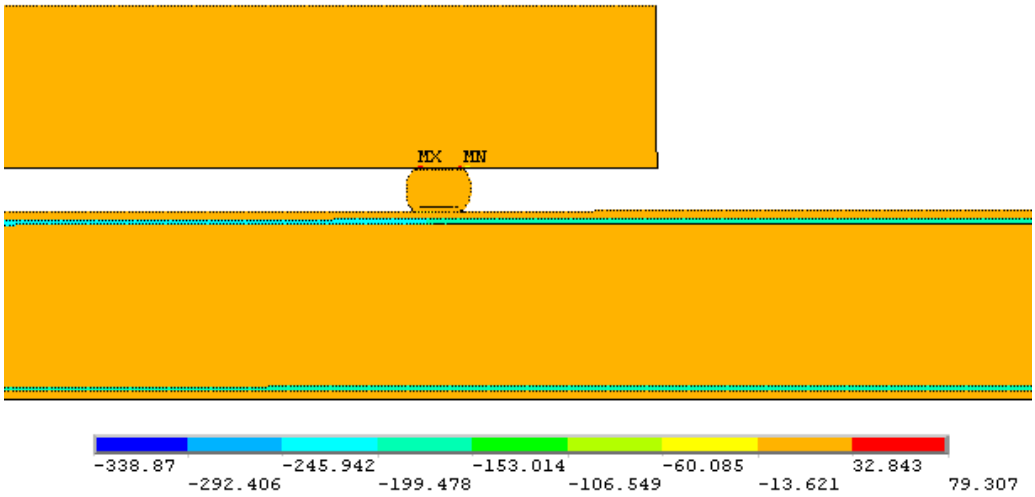


Figure 4.10 Stress induced in ABF/BT and RXP-1/RXP-4 at 150°C

After assembly, the RXP-4/RXP-1 system is found to develop much higher stress (Figure 4.12). This points to the need for an underfill to absorb some of the stress in order to successfully assemble ICs on thin substrates using this material system. Alternatively ACFs could be used for bonding.

ABF/BT



RXP-4/RXP-1

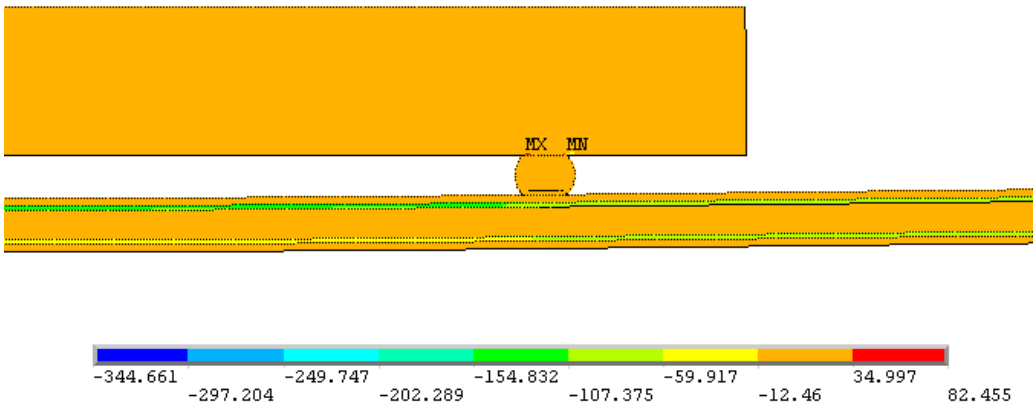
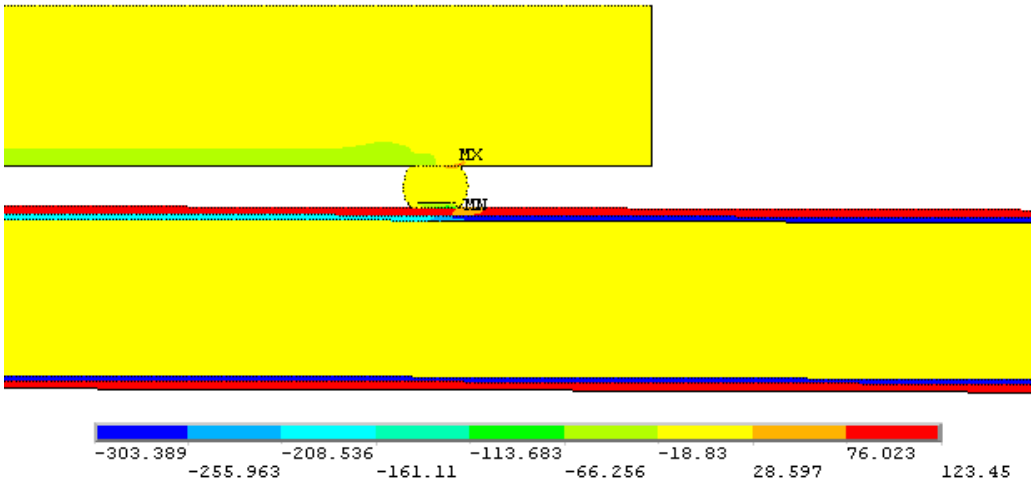


Figure 4.11 Stress induced in ABF/BT and RXP-1/RXP-4 at 240°C

ABF/BT



RXP-4/RXP-1

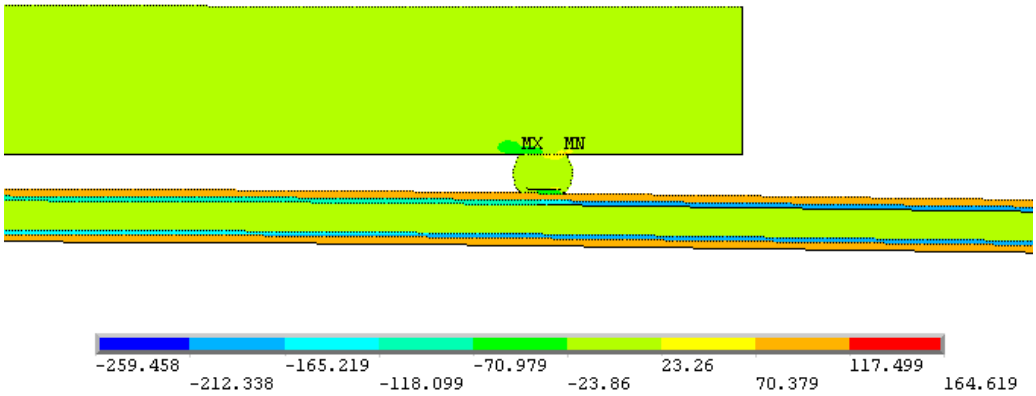


Figure 4.12 Stress induced in ABF/BT and RXP-1/RXP-4 at 25°C after assembly

4.6. Reliability of Ultra-Thin Substrates

The reduction in thickness of the substrate has a strong impact on reliability. Based on experimental and FEA data, it can be concluded that the reduction in thickness of the dielectric leads to increased microvia reliability for a given microvia diameter. This

could be attributed to stress concentration effects that arise as a result of a lower aspect ratio. It is found that the dielectric is the single most important factor affecting microvia reliability. The CTE of the dielectric should be as closely matched to copper to attain increased via reliability.

Warpage of ultra-thin substrates is found to increase as compared to a thick substrate. While this is a potential problem for assembly and reliability, the compliance of these substrates precludes some of these issues. The compliance of these substrates due to the low modulus and thickness of the substrate materials allows the film to flex and absorb stress. This allows the substrates to be assembled. Again, since the substrates can flex during reliability testing, ultra-thin substrates are found to be reliable.

4.7. Assembly on Thin Substrates

Due to the heavy warpage of these ultra-thin substrates, assembly was a concern. In order to show the feasibility of assembly on thin substrates, a 1 layer substrate was designed for assembly. Copper to copper bonding was performed using n-ACF. The pitch was 30µm. The thickness of the die is 500µm and the bump height is 10µm. This is shown in Figure 4.13.

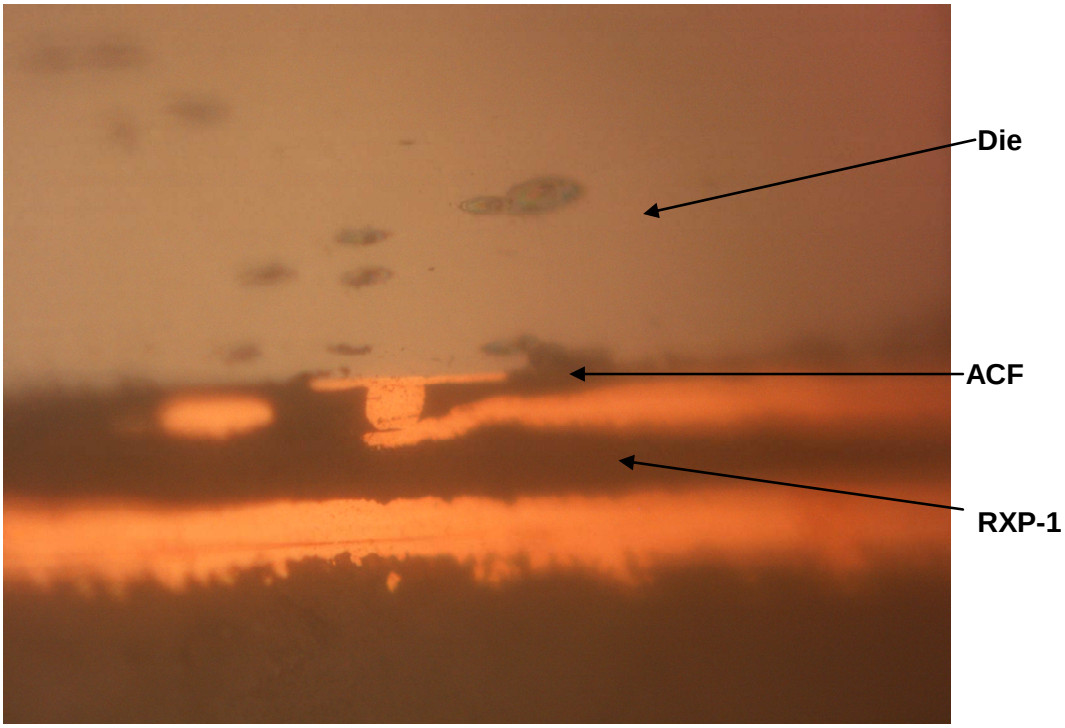


Figure 4.13 Optical micrograph of assembled die

It is found that the compliance of the substrate allows the die to be easily aligned and assembled on the substrate even at pitches as low as 30µm. Even though these ultra-thin substrates warp heavily, they are also flexible. They can be fixtured mechanically or using vacuum and then assembled.

CHAPTER 5

SUMMARY AND FUTURE WORK

This chapter is divided into two sections. The first section summarizes the work done and the conclusions that can be drawn from it. The second section explores the scope of future work

5.1. Summary

Miniaturization and functionality have always governed advances in electronic system technology. To truly achieve the goal of a multi mega-functional system, advances must be made not just at the IC level, but at the system level too. This concept of tighter integration at the system level is called System-on-Package (SOP). While SOP has a wide range of applications, this work targets the mobile application space. The main driver in the mobile application space is package profile. The reduction in thickness is a very critical for enabling ultra-high density mobile products for the next-generation. In order to pack more functionality into a smaller volume, it is absolutely imperative that package profiles are reduced.

Material properties play a very important role in the mobile application space. High frequency performance in the multiple-GHz range requires outstanding electrical properties in terms of dielectric constant and loss. Apart from the above factors, two other critical parameters required for advancing mobile technology are microvia and through

hole diameters. To support the spiraling need for higher wiring density, it is essential that microvia and through hole diameters are reduced.

This work explores a new material system with a low loss build-up dielectric core called RXP-4 and a low loss core called RXP-1. While new materials are critical for the continued advancement of system technology, reliable processes need to be developed for a new material set.

The main barriers to adoption of thin substrates come in the form of processing challenges, via and through hole reliability challenges and warpage. This work attempts to address these issues using new high-performance materials designed for high-frequency mobile applications.

Various processes were optimized on the new material system. The lamination of RXP-4 on RXP-1 was found to be a challenge. After extensive optimization, a reliable process was developed. Before optimization, the dielectric was found to blister on electroless plating. After optimization, this problem was solved. Research was then done on roughening the surface of the dielectric to enhance the reliability of the plated copper on the dielectric. Extensive process research was done to plate microvias and through holes.

A full fledged TV consisting of a 1+2+1 type stackup was then built to test for reliability. This TV consisted of microvia and through hole daisy chains. Microvia

diameters as low as 25µm and fine lines down to 15µm were demonstrated. Air-to-air thermal shock tests revealed excellent results. The microvias were found to survive for more than a 1000 cycles. About 2% of the vias were found to have failed after 1000 cycles.

FE modeling indicated similar results in terms of via reliability. Total strain ranges of the vias were estimated using FE modeling. This value was plugged into the Engelmaier relation to calculate an estimate for number of cycles to failure. The estimate was $> 10^5$ cycles.

Warpage was measured using Shadow Moiré and calculated using FE models. Similar trends were predicted by both experiments and modeling. Based on a stress analysis, it was concluded that assembly of ICs on thin substrates would be more reliable if an underfill were used. Assembly of a 30µm pitch die was then demonstrated using n-ACF.

5.2. Future Work

This work attempted to demonstrate the feasibility of using ultra-thin substrates for next-generation mobile applications. A number of other factors could be studied to provide a more comprehensive picture.

Via Filling

Via filling technology can be evaluated. A comparison can be made between filled vias and plated vias in terms of both electrical performance and thermo-mechanical reliability.

Drop Testing

Drop testing is an extremely important aspect of portable electronic products. Mechanical shock and vibration data would be very useful in this regard.

Comprehensive Warpage Assessment

While this work looked at warpage, the study was by no means comprehensive. A more complete warpage assessment should be performed to understand the effect of warpage on assembly and reliability. Direct relations could be derived between the reliability results and warpage after assembly.

REFERENCES

1. Tummala, R.R., *Moore's law meets its match (System-on-Package).* Spectrum, IEEE, 2006. **43**(6): p. 44-49.

2. Sundaram, V., et al., *Next-generation microvia and global wiring technologies for SOP.* Advanced Packaging, IEEE Transactions on [see also Components, Packaging and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on], 2004. **27**(2): p. 315-325.

3. *National Electronics Manufacturing Initiative (NEMI)*. 2007.

4. SIA Semiconductor Industry Association, A., VA, *Assembly & Packaging, The International Technology Roadmap for Semiconductors.* 2006.

5. Yu-Hua, C., et al. *Chip-in-substrate package, CiSP, technology*. 2004.

6. Towle, S.N., et al. *Bumpless Build-Up Layer Packaging*. 2001. New York, NY, United States: American Society of Mechanical Engineers.

7. Miller, H.S., *Intel's Vision of the Ultimate Package? Why It's the BBUL - No Package at All!* , in *Chip Scale Review*. 2002.

8. Young, T., M. Carano, and F. Polakovic, *Thermal reliability of high density interconnects utilizing microvias and standard through-hole technologies.* Circuit World, 1999. **26**(1): p. 22-26.

9. Young, T., F. Polakovic, and M. Carano. *Thermal reliability of laser ablated microvias and standard through-hole technologies as a function of materials and processing*. 2000. San Diego, CA, USA: IPC.

10. DiTomasso, J.D., *Stress analysis of vias with MCMs*, in *Mechanical Engineering*. 1996, University of Massachusetts at Amherst.

11. Prabhu, A.S., et al. *Thermo-mechanical fatigue analysis of high density interconnect vias*. 1995. Maui, HI, USA: ASME, New York, NY, USA.

12. Fuhan, L., et al., *Reliability assessment of microvias in HDI printed circuit boards.* Components and Packaging Technologies, IEEE Transactions on, 2002. **25**(2): p. 254-259.

13. Ramakrishna, G., L. Fuhan, and S.K. Sitaraman. *Experimental and numerical investigation of microvia reliability*. in *Thermal and Thermomechanical Phenomena in Electronic Systems, 2002. ITHERM 2002. The Eighth Intersociety Conference on*. 2002.

14. Dubey, A. *Effect of organic package warpage and assembly challenges using thin core substrate*. in *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th*. 2008.

15. Bhogeswara Rao, D. and M. Prakash. *Effect of substrate warpage on the second level assembly of advanced plastic ball grid array (PBGA) packages*. in *Electronics Manufacturing Technology Symposium, 1997., Twenty-First IEEE/CPMT International*. 1997.

16. Kumbhat, N., *New Carbon-Silicon Carbide Composite Board Material for High Density and High Reliability Packaging*, in *Materials Science and Engineering*. 2005, Georgia Institute of Technology.

17. Ratanawilai, T.B., et al., *A study on the variation of effective CTE of printed circuit boards through a validated comparison between strain gages and Moire´ interferometry.* Components and Packaging Technologies, IEEE Transactions on, 2003. **26**(4): p. 712-718.

18. Yu, Q., M. Shiratori, and Y. Ohshima. *A study of the effects of BGA solder geometry on fatigue life and reliability assessment*. in *Thermal and Thermomechanical Phenomena in Electronic Systems, 1998. ITHERM '98. The Sixth Intersociety Conference on*. 1998.

19. Michaelides, S. and S.K. Sitaraman. *Effect of material and geometry parameters on the thermo-mechanical reliability of flip-chip assemblies*. in *Thermal and Thermomechanical Phenomena in Electronic Systems, 1998. ITHERM '98. The Sixth Intersociety Conference on*. 1998.

20. Shang, J. and Y.-I. Liu, *New materials and challenges in build-up, RF and high speed applications - An overview.* Circuit World, 2003. **29**(4): p. 28-33.

21. Banerji, S., *Warpage characterization and lithographic limitations of FR-4 for SOP global interconnect needs*, in *School of Materials Science and Engineering*. 2002, Georgia Institute of Technology.

22. Mahalingam, S., et al. *Materials, processes and reliability of mixed-signal substrates for SOP technology*. in *Electronic Components and Technology Conference, 2004. Proceedings. 54th.* 2004.

23. Kumbhat, N., et al. *Next generation of package/board materials technology for ultra-high density wiring and fine-pitch reliable interconnection assembly*. in *Electronic Components and Technology Conference, 2004. Proceedings. 54th.* 2004.

24. Hai, D., et al., *Warpage measurement comparison using shadow Moire and projection Moire methods.* Components and Packaging Technologies, IEEE Transactions on, 2002. **25**(4): p. 714-721.